HP 7902A Disc Drive

Preliminary Service Manual

HEWLETT PACKARD

HP 7902A
DISC DRIVE

PRELIMINARY
SERVICE MANUAL

Manual part no. 07902-90060

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LIST OF EFFECTIVE PAGES

New editions of this manual will incorporate all material updated since the previous edition. Update packages may be issued between editions and contain replacement and additional pages to be merged into the manual by the user. Each updated page will be indicated by a revised date at the bottom of the page. A vertical line in the outer margin on each page indicates where changes occur. Note that pages which are rearranged due to changes on a previous page are not considered revised.

The manual printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates which are incorporated at reprint do not cause the date to change.) The manual part number changes when extensive technical changes are incorporated.

August 1978....**First Edition**

May 1979....Updated pages: vii, ix, 7-4, 7-11 thru 7-16, 9-16 thru 9-18.

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SAFETY CONSIDERATIONS

KEEP WITH MANUAL

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

SECTION I
GENERAL DESCRIPTION

1-1. INTRODUCTION

This section contains a general description of the HP 7902A Disc Drive, and specifications.

1-2. GENERAL DESCRIPTION

The HP 7902A Flexible Disc Drive is a random-access data storage system employing a flexible medium. The HP 7902A consists of a controller printed-circuit assembly (PCA), a disc drive assembly, and a drive PCA. All necessary operating voltages must be provided by the host system. The controller PCA accepts and interprets commands over the Hewlett-Packard Interface Bus (HP-IB), controls the interface to the disc drive assembly, stores and retrieves data from the disc drive assembly, and returns disc drive and disc operation status information. The drive PCA is mounted in the disc drive assembly and contains read and write circuits, interlocks, and head positioning and head load circuits. The remainder of the drive electronics circuitry is located on the separately-mounted controller PCA.

The flexible medium used in the HP 7902A is a flexible disc, commonly called a diskette. The flexible disc is 20 centimeters (7.9 inches) in diameter and has a 3.8-centimeter (1.5-inch) hole for alignment on the spindle of the disc drive. The disc is enclosed in a protective polyvinyl-chloride (PVC) jacket with a slot for head access to the recording surface. Both sides of the flexible disc are used for data storage.

The recording head in the disc drive assembly is positioned by a mechanism that includes a stepper motor, capstan, and taut metal band. The mechanism operates in an open loop configuration — there is no positive feedback to determine the actual position of the head. The recording head has two read/write heads, one for each side of the flexible disc. When the heads are loaded, both contact the media. The heads remain loaded for approximately one second after no further commands are received.

The controller PCA contains a micro CPU chip (MC^2), a processor-to-HP-IB interface (PHI) chip, read-only memory (ROM), random access memory (RAM), and the associated logic circuits necessary to provide an interface between up to four disc drive assemblies and the HP-IB interface channel. The MC^2 handles data and commands directly at the byte level, eliminating the need for direct-memory access (DMA) hardware.

The controller PCA also contains an extensive self-test capability, including options for reading from an already formatted flexible disc and reading and writing on a previously unformatted disc. All self-test functions except reading from a previously formatted disc may be initiated via HP-IB command or by manual switching. The preformatted read self-test is switch initiated. The controller PCA performs a subset of self-test each time power is applied to the HP 7902A. This subset does not include reading or writing on the flexible disc. Self-test results are available as a four-bit binary word displayed on an LED array mounted on the controller PCA or as two bytes of status information which can be read by the host system.

The HP 7902A will read and write the HP standard flexible disc format as used on the HP 9885 Flexible Disc Drive on either single-sided or double-sided flexible discs. The HP 7902A will also read and write the IBM 128 byte/sector standard data interchange format on single-sided flexible discs only. When a new (previously formatted) flexible disc is loaded into the disc drive, the controller PCA will determine which format is being used and whether the disc is single- or double-sided. Format and disc type are both reported as status information. When a disc is reformatted, the controller PCA performs defective track sparing and track reformatting.

Data transfers can be buffered on a sector-to-sector basis. This allows devices connected to the HP 7902A to access data at any rate up to the maximum burst rate. Unbuffered data transfers may also be done, but this requires that the devices accept data at the rate that the HP 7902A sends it.

A modular replacement philosophy has been implemented in the HP 7902A to minimize on-site repair time. Troubleshooting the HP 7902A is simplified by its self-test diagnostics. In addition, more extensive diagnostic testing using automatic test equipment connected to the controller PCA is possible. These diagnostics are not described in this manual since they are a function of the host system.

1-3. SPECIFICATIONS

Table 1-1 lists specifications for the HP 7902A Disc Drive.

Table 1-1. HP 7902A Specifications

RECORDING SPECIFICATIONS

HP DOUBLE DENSITY FORMAT

Encoding:	M^2FM
Rotational Speed:	360 RPM ± 3.5% (±12.6 RPM)

Bit Density @ 360 RPM:

Track No.	Head 0 (Single/Double-sided)	Head 1 (Double-sided only)
0	3651 FRPI*	3736 FRPI
38	4702	4845
76	6813	7023

* FRPI — Flux reversals per inch.

Track Density:	48 tracks per inch
Tracks per surface:	77
Surfaces per disc:	2

IBM SINGLE DENSITY FORMAT

Encoding:	FM
Rotational Speed:	360 RPM ±1% (± 3.6 RPM)
Bit Density @ 360 RPM:	3200 FRPI, track 76, head 0
Track Density:	48 tracks per inch
Tracks per surface:	77
Surfaces per disc:	1

Table 1-1. HP 7902A Specifications (Continued)

CAPACITY

HP DOUBLE DENSITY FORMAT

Bytes/Sector:	256
Sectors/Track:	30
Tracks/Surface:	154 on two surfaces
Bytes/Drive (Formatted):	1.18 Mbytes (154 tracks)

IBM SINGLE DENSITY FORMAT

Bytes/Sector:	128
Sectors/Track:	26
Tracks/Surface:	77 (Head 0 only)
Bytes/Drive (Formatted):	256 kbytes

ACCESS TIME

Track-to-Track Seek:	3 msec/track, plus 15 msec settling
Maximum Track-to-Track Seek (77 tracks):	246 msec
Average Track-to-Track Seek:	91 msec
Maximum Rotational Latency:	167 msec
Average Rotational Latency:	88 msec
Maximum Data Access Time (Seek plus Latency):	413 msec
Average Data Access Time:	174 msec

DATA TRANSFER RATE

BUFFERED MODE

Read Burst Transfer Rate:	135 kbytes/sec
Write Burst Transfer Rate:	110 kbytes/sec
HP Format Average Transfer Rate (Note 1):	23 kbytes/sec
IBM Format Average Transfer Rate (Note 2):	10 kbytes/sec

Note 1: Staggering parameter dependent — best case every other sector.

Note 2: Staggering parameter dependent — best case every other sector. If sectors are not staggered then only one sector per revolution can be transferred in buffered mode — 768 bytes/sec.

Table 1-1. HP 7902A Specifications (Continued)

UNBUFFERED MODE

HP Format:	46 kbytes/sec avg, 62 kbytes/sec max (Note 3)
IBM Format:	20 kbytes/sec avg, 31 kbytes/sec max (Note 3)

Note 3: Average transfer rate based on total number of data bytes/second; maximum transfer rate based on a write frequency of 500 kHz for HP format and 250 kHz for IBM format.

ENVIRONMENTAL SPECIFICATIONS

OPERATING LIMITS

Temperature:	10°C to 40°C (50°F to 104°F)
Relative Humidity:	20% to 80% with maximum wet bulb temperature not to exceed (non-condensing) 25.5°C (77.9°F)
Altitude:	0 to 4 572 m (0 to 15,000 ft)

NON-OPERATING LIMITS (STORAGE AND TRANSIT)

Temperature:	−40°C to 60°C (−40°F to 140°F)
Altitude:	−304.8 to 15 240 m (−1,000 to 50,000 ft)

ALIGNMENT LIMITS

Radial Alignment:	± 0.001 inch of track center at track 38 for both head 0 and head 1

POWER REQUIREMENTS

CONTROLLER PCA

+5V:	2.5A typical, 2.7A maximum (Note 4)
+12V:	0.25A typical, 0.30A maximum (Note 5)
−12V:	0.08A typical, 0.1A maximum (Note 5)

DRIVE PCA

+5V:	0.6A typical, 0.7A maximum (Note 4)
+12V:	0.8A typical, 1.0A maximum (Note 5)
−12V:	0.8A typical, 1.0A maximum (Note 5)

Note 4: Voltage tolerance for +5V is +5%, −3%.

Note 5: Voltage tolerance for +12V and −12V is ±5%.

Table 1-1. HP 7902A Specifications (Continued)

DISC DRIVE ASSEMBLY

86 to 127 Vac at 0.3A typical, 0.44A maximum
50/60 Hz ± 3.5% HP format
50/60 Hz ± 1% IBM format

MEDIA LIFE

Revolutions:	> 3 (10^6) on any track, heads loaded.
Insertions:	> 30,000

HEAD LIFE

More than 15,000 hours of operation with use of HP approved media.

SECTION II
INTERFACE INFORMATION

2-1. INTRODUCTION

This section provides information required to interface the HP 7902A Disc Drive with a host system. Included are dimensions, power requirements, cabling data, switch settings, environmental limitations, and design details for a front panel display.

2-2. DIMENSIONS

Dimensions for the 07902-60025 disc drive assembly are shown in figure 2-1.

2-3. POWER REQUIREMENTS

Power requirements for the HP 7902A Disc Drive components are listed in table 2-1.

2-4. POWER SEQUENCING

Power On signal PON should stay low until well after all dc supply voltages have stabilized (greater than 100 milliseconds). Signal PON should go low immediately if ac power is not within specifications, or if dc power is about to fail.

System Reset ($\overline{\text{SYSRST}}$) is a logic level, active low, signal which performs the same function as PON for the controller. It forces the system to First Status state. (Refer to paragraph 4-23 for additional information.)

AC power must be within specification for at least two seconds before reading and/or writing. This is to allow the spindle rotational speed to stabilize.

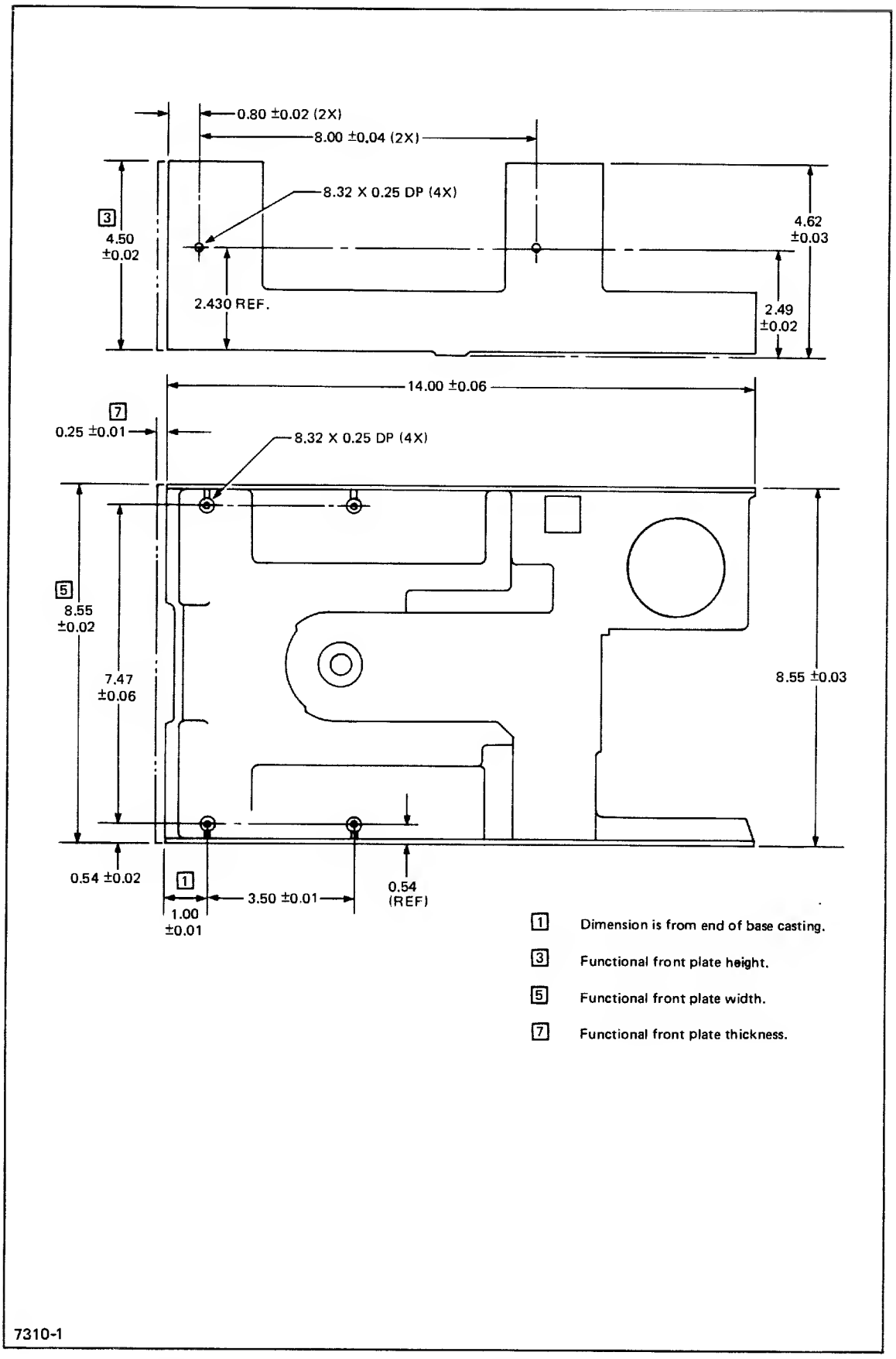


Figure 2-1. Disc Drive Assembly (07902-60025) Dimensions

Table 2-1. HP 7902A Disc Drive Power Requirements

CONTROLLER PCA-A1 (07902-60024)

+5V 2.5A typical, 2.7A max, voltage tolerance: +5%, −3%
+12V 0.25A typical, 0.30A max, voltage tolerance: ±5%
−12V 0.08A typical, 0.1A max, voltage tolerance: ±5%

DRIVE PCA-A2 (07902-60023)

+5V 0.6A typical, 0.7A max, voltage tolerance: +5%, −3%
+12V 0.8A typical, 1.0A max, voltage tolerance: ±5%
−12V 0.8A typical, 1.0A max, voltage tolerance: ±5%

DISC DRIVE ASSEMBLY (07902-60025)

86 – 127 Vac at 0.3A typical, 0.44A max
50/60 Hz ±3.5% HP Format
50/60 Hz ±1% IBM Format

2-5. COOLING REQUIREMENTS

The operating limits of the 07902-60025 disc drive assembly and medium are specified as 10°C to 40°C, 20 to 80 percent relative humidity (RH) with maximum wet-bulb temperature of 25.5°C. These limits allow for a rise in the disc drive of 10°C. The actual operating limits are set by the medium. IBM sets the limits at 10°C to 52.6°C, 8 to 80 percent RH, maximum wet-bulb temperature of 29.4°C.

2-6. SHIELDING REQUIREMENTS

No shielding is required under normal operating conditions. If the disc drive assembly is subjected to medium- to high-intensity electromagnetic fields such as those from the yoke of a cathode-ray tube, an aluminum or steel shield should be placed between the source of the field and the disc drive. The head load solenoid has a small dc external field that may cause CRT deflection. A steel shield wrapped around the disc drive assembly will eliminate this source of interference.

2-7. HARDWARE INTERFACE

The HP 7902A consists of three major assemblies: controller PCA-A1, part no. 07902-60024; drive PCA-A2, part no. 07902-60023; and disc drive assembly, part no. 07902-60025. Details of the interface cabling between these items are as follows.

Figure 2-2 shows the location of the front and rear edge connectors on controller PCA-A1 and table 2-2 lists the pin assignments for these connectors. Connection to the HP-IB is through 26-pin connector A1J3. Connectors A1J1 and A1J2 are reserved for test purposes. Connection to drive PCA-A2 is via 50-pin connector A1P1. Connectors A1P2, A1P3, and A1P4 are used for host system power and power sequencing connections.

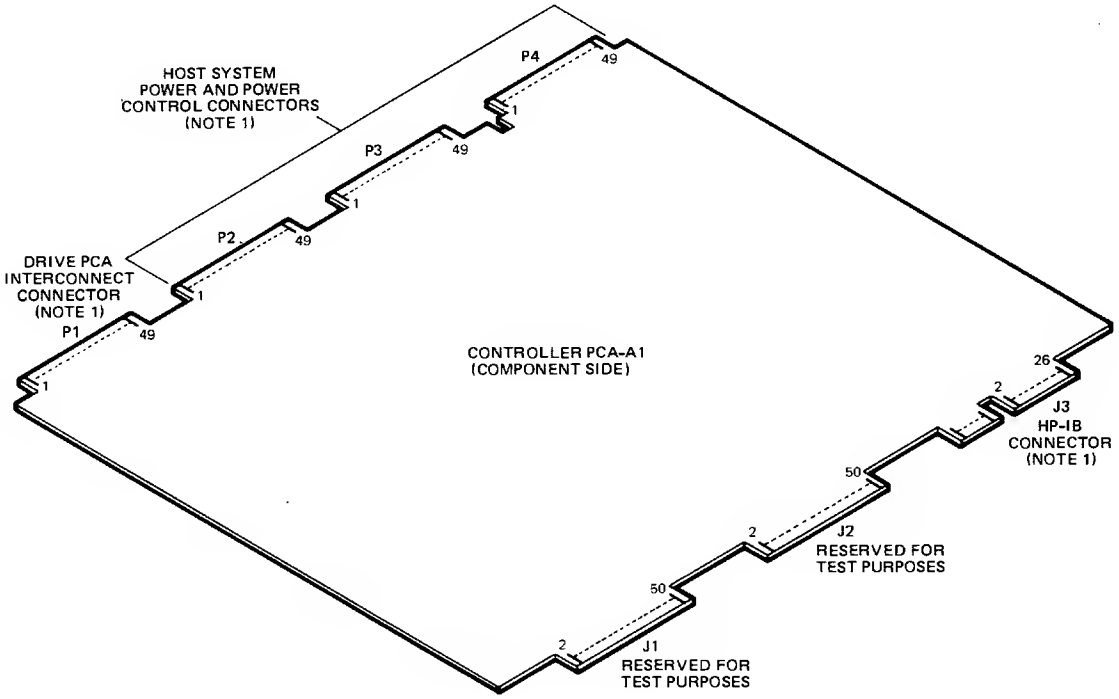
Figure 2-3 shows the location of the connectors on drive PCA-A2. Connection to controller PCA-A1 is through 50-pin connector A2J1. DC power is connected via A2J5. Table 2-3 lists the pin assignments for connectors A2J1 and A2J5. Interface to the disc drive is via connectors A2J2, A2J3, and A2J7. Power for the DSU is supplied by connector A2J8. Connections for a disc drive display panel are provided by connector A2J6 (refer to paragraph 2-8 for details).

AC power for the disc drive assembly is connected directly to a 3-pin connector, located on the drive, between the actuator and the spindle motor capacitor. See figure 2-4. Pin assignments for the connector are as follows:

Pin	Signal
1	ac line
2	frame ground
3	ac neutral

Mating parts for the connector are:

Body, part no. 1251-3913 (Amp 1-480700-0)
Pin, part no. 1251-3915 (Amp 350547-1)



NOTE 1: REFER TO TABLE 2-2 FOR PIN ASSIGNMENTS.

7310-2

Figure 2-2. Controller PCA-A1 (07902-60024) Connectors

Table 2-2. Controller PCA-A1 (07902-60024) Connector Pin Assignments

A1P1 (See Notes 1 and 3)

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	DSL0H
3	GND	4	DSL1H
5	GND	6	DSL2H
7	GND	8	DSLVL
9	GND	10	LDCTL
11	GND	12	STENL
13	GND	14	RSPNH
15	GND	16	WRITL
17	GND	18	PHIBH
19	GND	20	PHIAH
21	GND	22	DLCKL
23	GND	24	HED1H
25	GND	26	PORH
27	GND	28	INDXL
29	GND	30	SPINL
31	GND	32	TRK0L
33	GND	34	WPRTL
35	GND	36	REDYH
37	GND	38	DATAH
39	GND	40	DATAL
41	GND	42	NC
43	KEY	44	KEY
45	GND	46	NC
47	GND	48	PONH
49	GND	50	−5V TP

A1J3 (See Note 2)

PIN	SIGNAL	PIN	SIGNAL
1	NC	2	NC
3	GND	4	GND (Shield)
5	GND	6	ATN
7	GND	8	SRQ
9	GND	10	IFC
11	GND	12	NDAC
13	GND	14	NRFD
15	GND	16	DAV
17	REN	18	EOI
19	DIO8	20	DIO4
21	DIO7	22	DIO3
23	DIO6	24	DIO2
25	DIO5	26	DIO1

A1P2 (See Notes 1 and 4)

PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	+5V
3	+5V	4	+5V
7	−12V	8	−12V
13	+12V	14	+12V
17	NC	18	GND
27	NC	28	GND
35	GND	36	PON
45	GND	46	GND

A1P4 (See Notes 1 and 4)

PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	+5V
3	+5V	4	+5V
7	−12V	8	−12V
13	+12V	14	+12V
17	NC	18	GND
27	NC	28	GND
33	$\overline{\text{SYSRST}}$	34	NC
35	GND	36	PON
45	GND	46	GND

Notes:

1. Even-numbered pins are on circuit side of PCA, odd-numbered pins are on component side.
2. Odd-numbered pins are on circuit side of the PCA, even-numbered pins are on component side.
3. Refer to table 6-1 for definitions of the signal mnemonics.
4. Signals PON and $\overline{\text{SYSRST}}$ are described in paragraph 2-4.

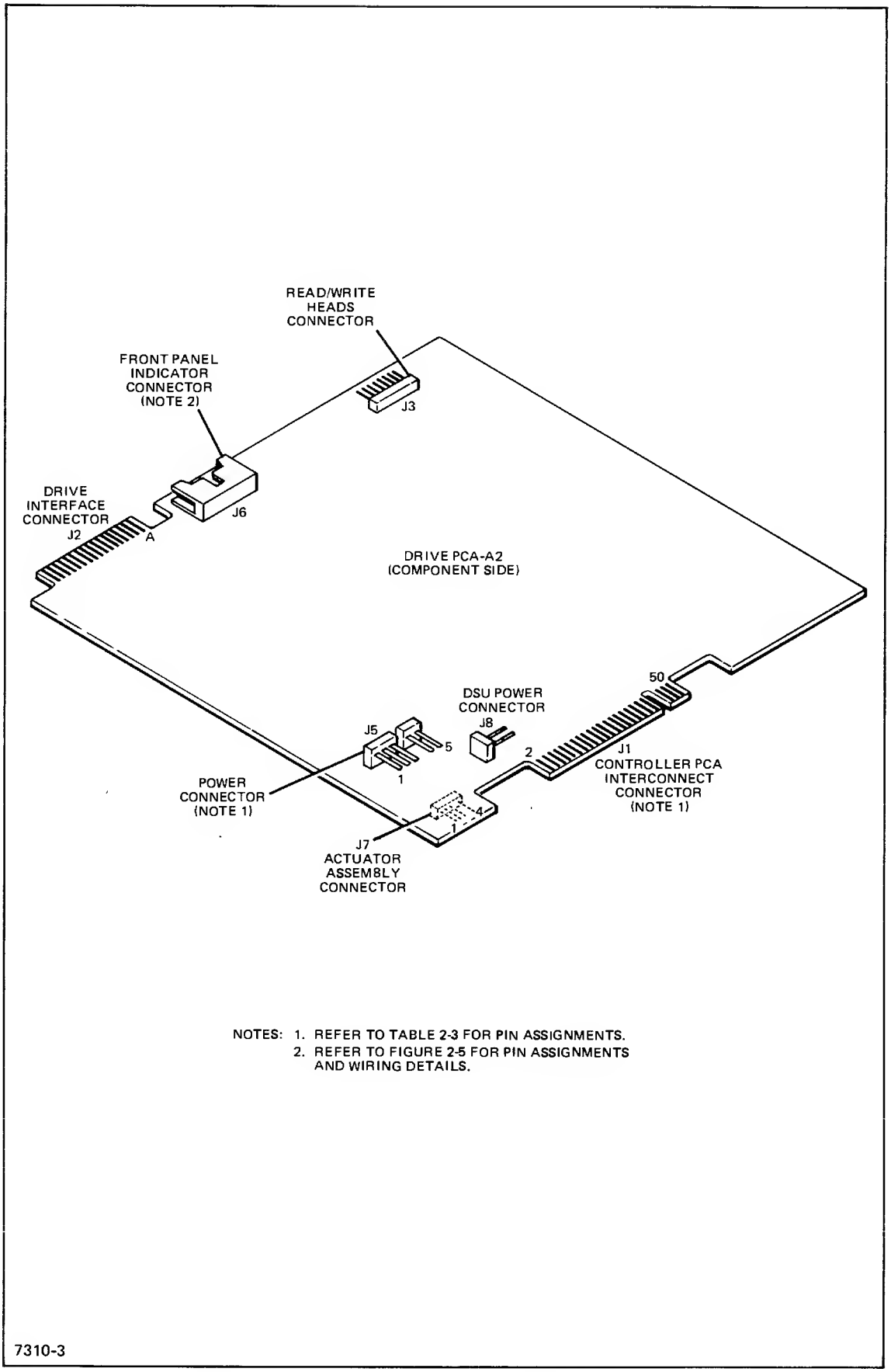


Figure 2-3. Drive PCA-A2 (07902-60023) Connectors

Table 2-3. Drive PCA-A2 (07902-60023) Connector Pin Assignments

A2J1 (See Notes 1 and 3)

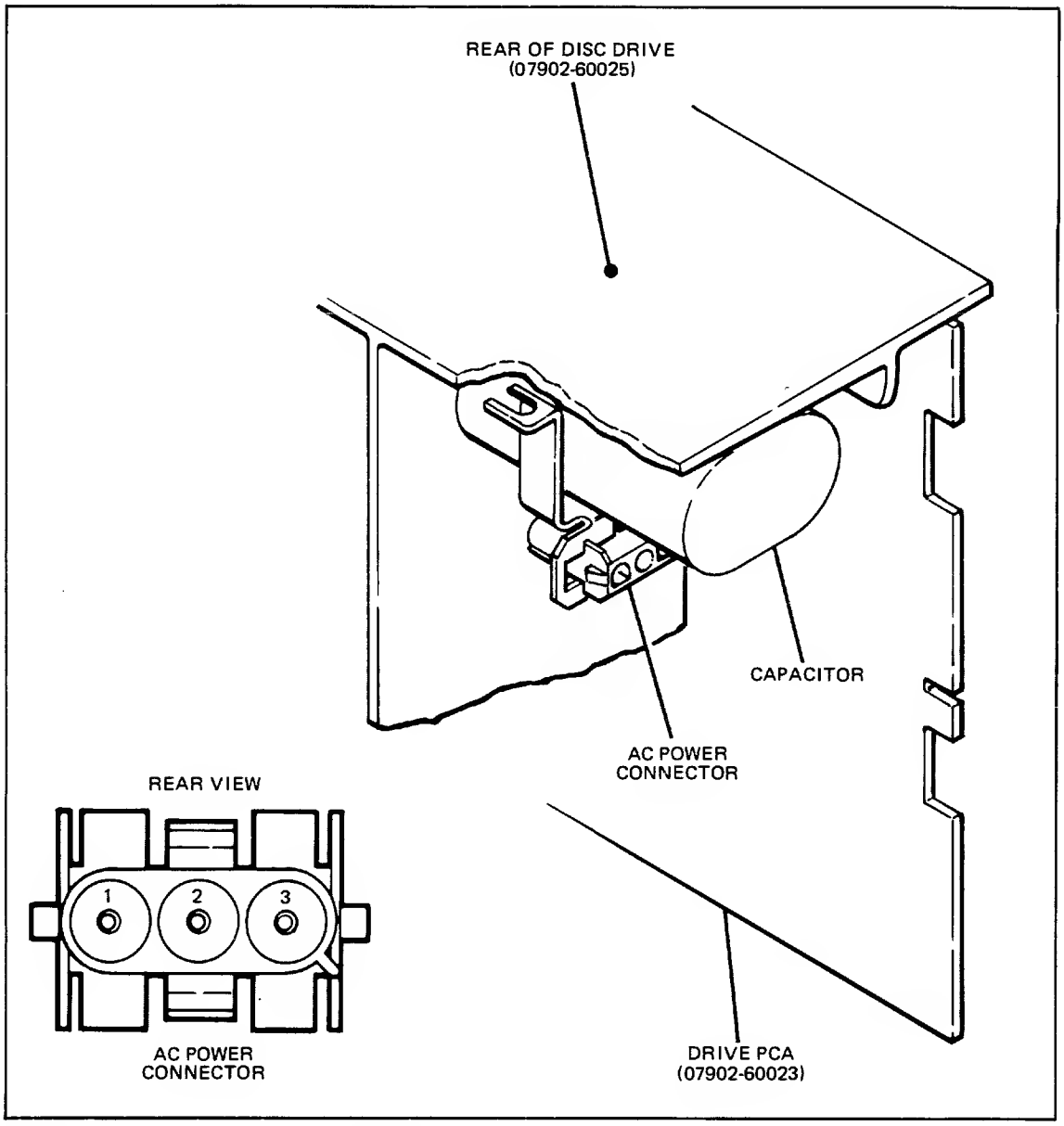
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	DSL0H
3	GND	4	DSL1H
5	GND	6	DSL2H
7	GND	8	DSLVL
9	GND	10	LDCTL
11	GND	12	STENL
13	GND	14	RSPNH
15	GND	16	WRITL
17	GND	18	PHIBH
19	GND	20	PHIAH
21	GND	22	DLCKL
23	GND	24	HED1H
25	GND	26	PORH
27	GND	28	INDXL
29	GND	30	SPINL
31	GND	32	TRK0L
33	GND	34	WPRTL
35	GND	36	REDYH
37	GND	38	DATAH
39	GND	40	DATAL
41	GND	42	NC
43	KEY	44	KEY
45	GND	46	NC
47	GND	48	PONH
49	GND	50	−5V TP

A2J5 (See Note 2)

PIN	SIGNAL
1	GND
2	GND
3	+12V
4	KEY
5	−12V
6	+5V

Notes:

1. Odd-numbered pins are on circuit side of the PCA, even-numbered pins are on component side.
2. A2J5 mating connector: part no. 1251-3275 (Molex 09-50-7061)
   A2J5 connector contacts: part no. 1251-0670 (Molex 08-50-0105)
   A2J5 connector key: part no. 1251-0627 (Molex 15-04-0219)
3. Refer to table 6-1 for definitions of the signal mnemonics.

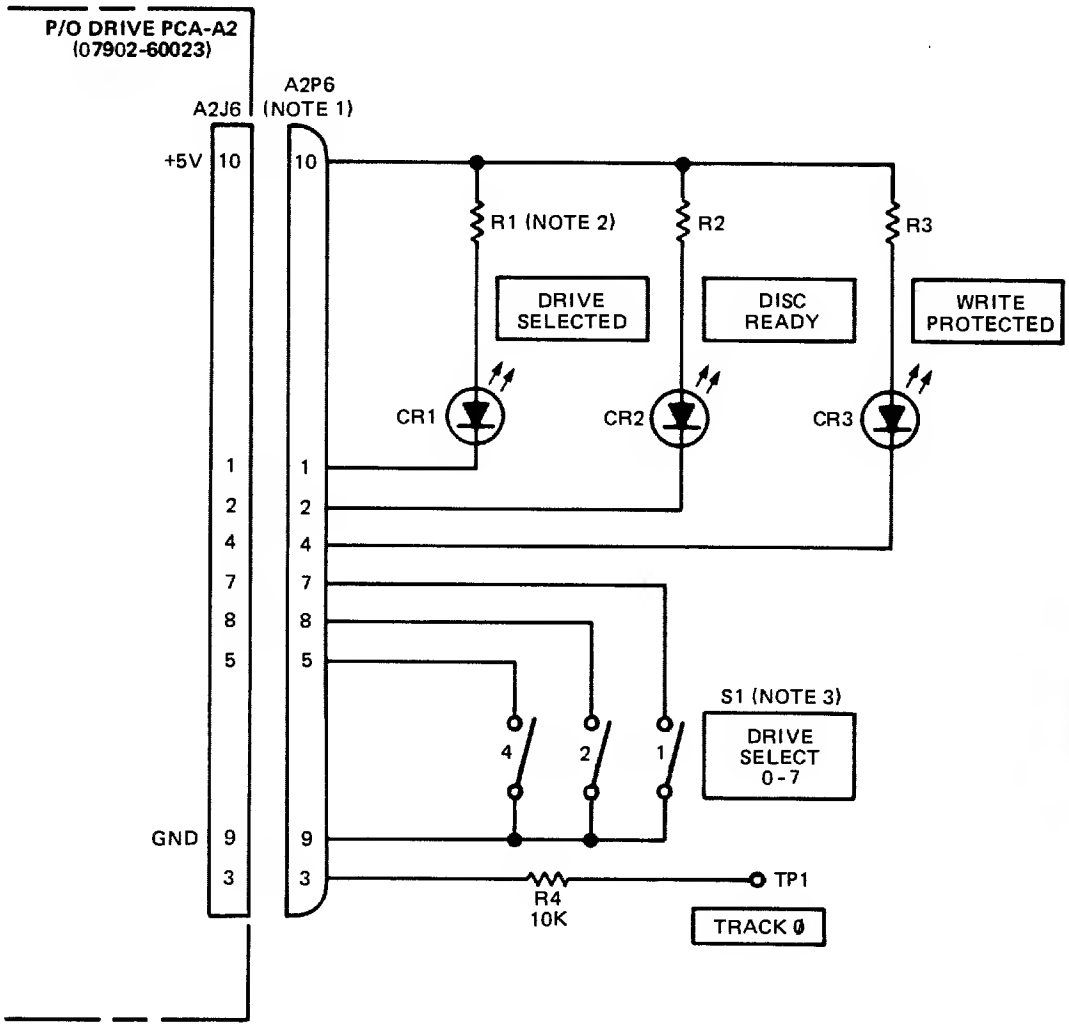


7310-4

Figure 2-4. AC Power Connector

2-8. FRONT PANEL INDICATOR DISPLAY

Connector A2J6 on drive PCA-A2 (see figure 2-3) is available for displaying disc drive status and for disc drive number selection. A typical design for a front panel indicator display employing the data available at A2J6 is shown in figure 2-5. If no DRIVE SELECT switch is connected to A2J6, drive select will default to number 0. The LED status indicators shown in the design are driven by low-power Schottky buffers (active low). The LED current should be limited to 20 milliamperes or less.



NOTES:
1. A2P6 IS A 10-PIN RIBBON CONNECTOR, HP PART NO. 1251-4006 (3M, PART NO. 3473-0000).
2. LED'S CR1 THROUGH CR3 ARE DRIVEN BY LOW-POWER SCHOTTKY BUFFERS (ACTIVE LOW). LIMIT LED CURRENT TO 20 mA OR LESS.
3. S1 IS A BINARY ENCODED 1 OF 8 SWITCH, LOW TRUE. A TYPICAL PC MOUNT THUMBWHEEL SWITCH IS HP PART NO. 3100-3395 (EECO, PART NO. 1A-21-50-61G).

7310-5

Figure 2-5. Typical Front Panel Indicator Display

2-9. CONTROLS

There are three switches, an LED display, and two test pins on the front edge of controller PCA-A1. See figure 2-6. These controls are described in the following paragraph. There are no controls on the disc drive assembly or drive PCA-A2.

The thumbwheel switch on the front right of controller PCA-A1, next to connector A1J1 (HP-IB connector) is the HP-IB switch. Each time controller PCA-A1 is powered up, cleared, or reset, the value set on the switch is loaded into the HP-IB interface chip (PHI) before the PHI is put on line. The HP-IB address range is 0 – 7. The two momentary close switches, LED display, and two test pins on the front of controller PCA-A1 are used for self-test control and readout. The functions of these components are fully described in section VIII of this manual.

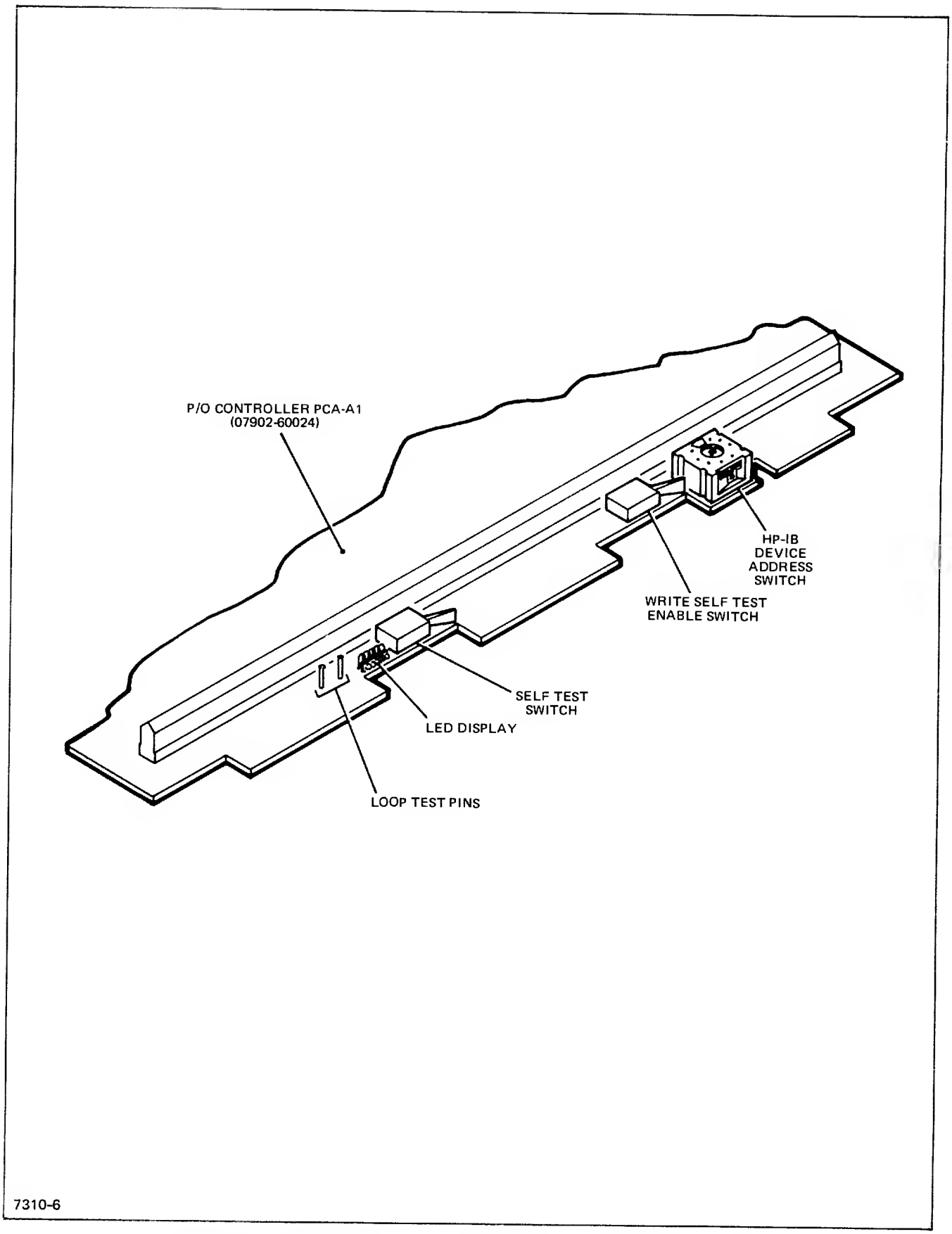


Figure 2-6. Controller PCA-A1 (07902-60024) Controls and Indicators

SECTION III
OPERATION

3-1. INTRODUCTION

This section contains flexible disc (diskette) loading instructions, flexible disc handling precautions, and details of the disc drive write protect capability.

3-2. FLEXIBLE DISC LOADING

Figure 3-1 shows the proper method of loading the flexible disc into the disc drive. To load a disc, proceed as follows.

Note: Disc loading/unloading can occur with disc drive power on and the drive spindle rotating.

a. Open the door on the front of the drive by pressing in on the door latch.

b. Insert the disc into the drive, with the label on the disc facing right, as shown in figure 3-1.

c. Move the latch handle to the right until it locks in place.

3-3. FLEXIBLE DISC HANDLING PRECAUTIONS

The flexible disc is enclosed in a plastic jacket which is lined with a wiping material that cleans the disc of foreign matter. When not in use, the disc should always be stored in its protective envelope. To ensure error-free disc drive operation, the following additional precautions should be observed.

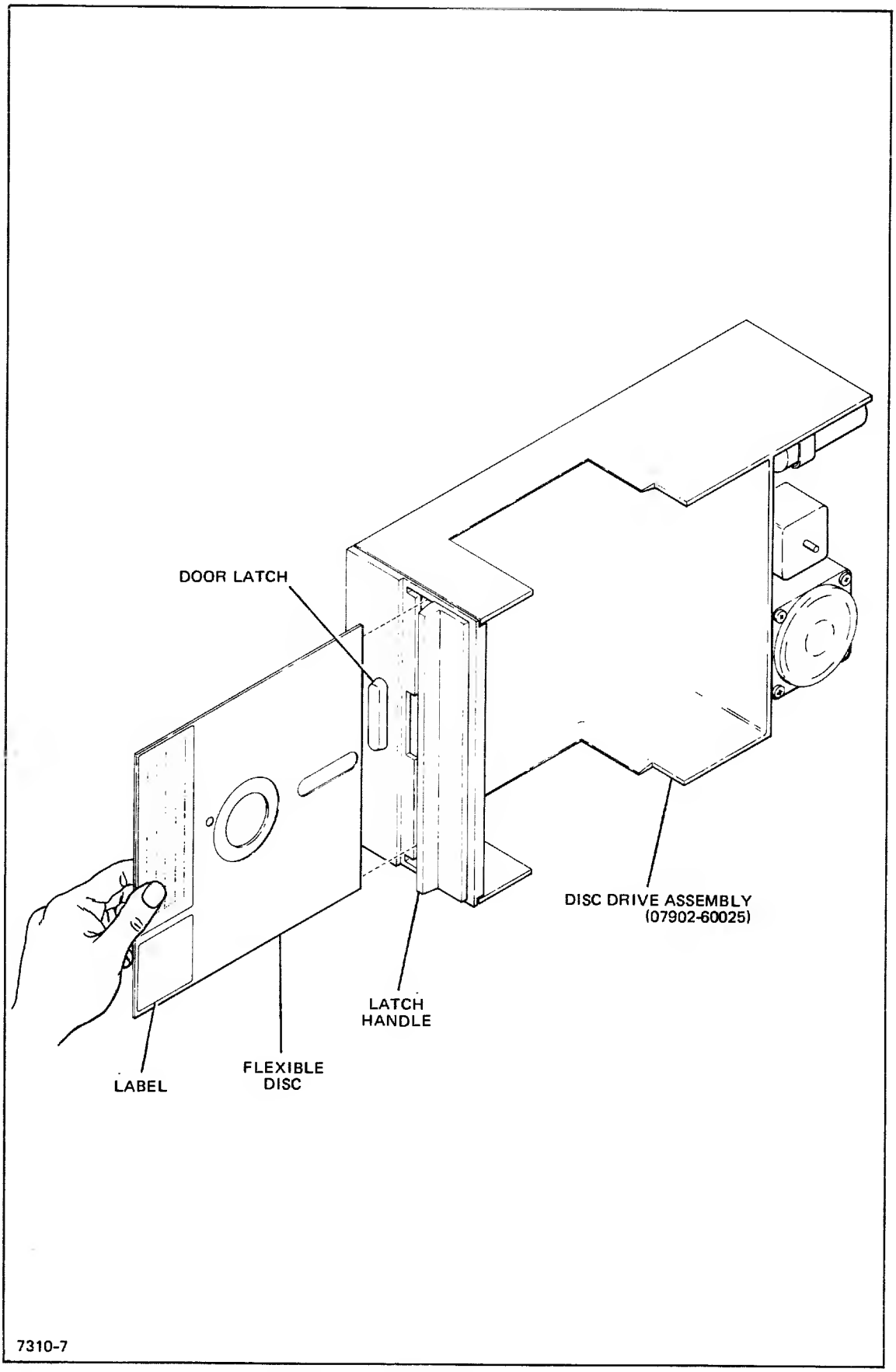


Figure 3-1. Flexible Disc Loading Details

- Use only HP-approved flexible discs. Use of any others can result in damage to the drive mechanism, high maintenance costs, and data loss. HP warranty does not cover damage caused by the use of flexible discs not approved by HP.

- Return the disc to its storage envelope whenever it is removed from the disc drive.

- Replace storage envelopes when they become worn, cracked, or distorted.

- Do not touch or attempt to clean the surface of the disc. Abrasions may cause the loss of stored data.

- Do not write on the plastic jacket of the disc with a lead pencil or ballpoint pen. Use a felt-tip pen and write only on the label.

- Do not expose the disc to extremes of temperature and/or humidity. (Disc drive environmental limitations are listed in table 1-1.)

- Keep the flexible discs away from magnetic fields and ferromagnetic materials that may become magnetized. Strong magnetic fields can distort the data recorded on a disc.

3-4. WRITE PROTECT

The flexible disc has the capability of being write protected. This feature prevents the accidental erasure of data recorded on the disc. The write protect feature is enabled when the write protect notch on the cover of the flexible disc (see figure 3-2A) is uncovered. When the notch is covered, writing is allowed on the disc.

The write protect notch may be covered by placing a tab over the notch on the top side of the disc jacket and then folding the tab over the edge to cover the notch on the bottom side. The installation of the tab is shown in figure 3-2A.

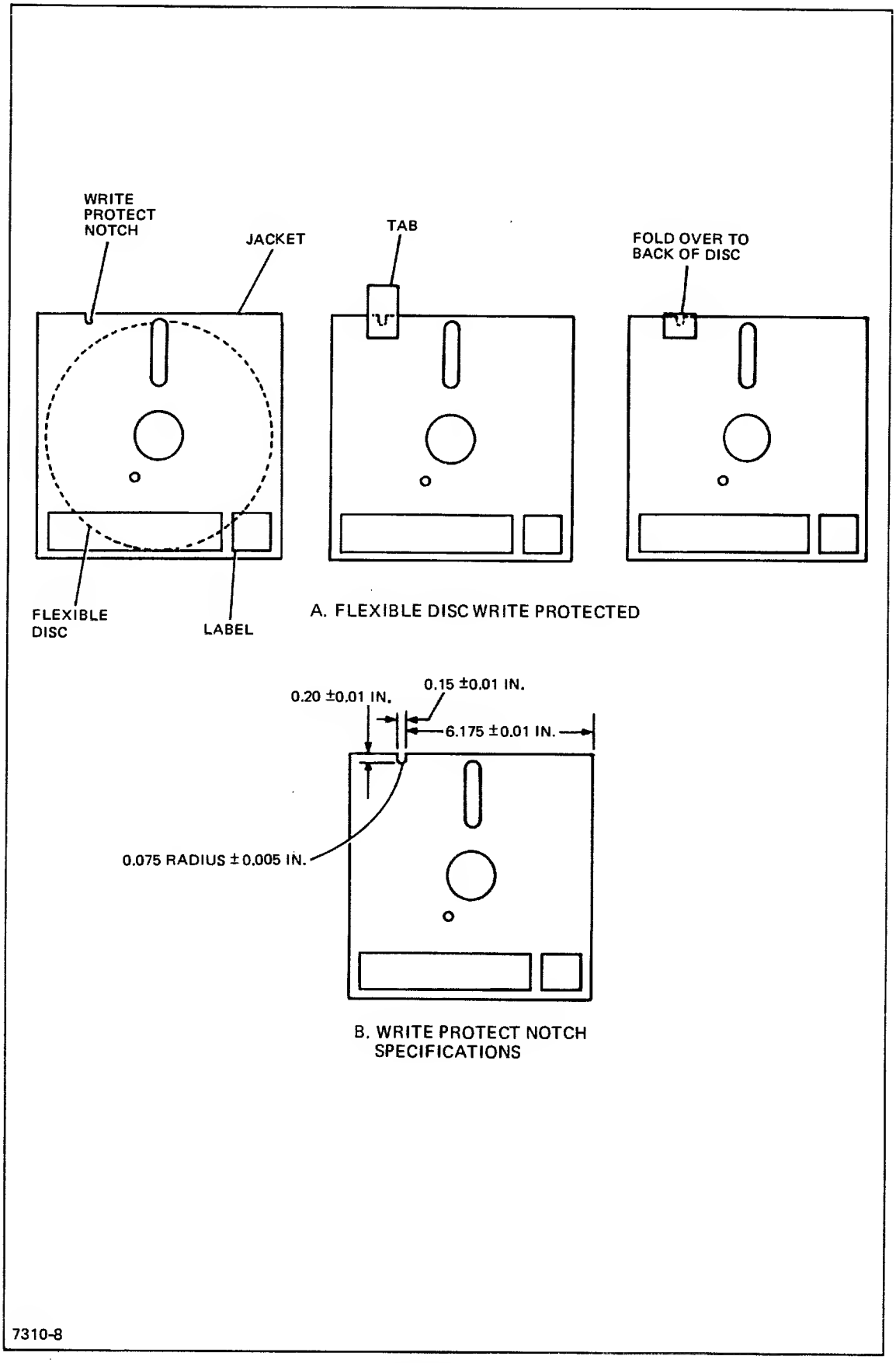


Figure 3-2. Write Protect Details

Certain HP-approved flexible discs may not have a write protect notch. To write protect such a disc, a notch may be cut in the jacket following the dimensions given in figure 3-2B. A tool, part no. T-196432, is available for this purpose.

3-5. OPERATOR CONTROLS

There are no operator controls on the HP 7902A Disc Drive.

SECTION IV
FUNCTIONAL CHARACTERISTICS AND COMMUNICATION PROTOCOL

4-1. INTRODUCTION

This section describes the recording formats used in the HP 7902A, and the HP 7902A command set.

4-2. RECORDING FORMATS

The HP 7902A Disc Drive supports both the HP standard flexible disc format (hereafter referred to as the HP format) and the IBM standard data interchange format (hereafter referred to as the IBM format). Many basic features of both formats are identical and many are different. Format similarities and differences are described in the following paragraphs.

4-3. FORMAT SIMILARITIES

The following features are common to both the IBM format and the HP format.

4-4. MEDIA. A double-sided flexible disc (diskette) is used as the recording medium. The disc is composed of flexible recording material and is enclosed in a square plastic jacket. An index hole in the disc is used to provide a rotational position reference. The disc drive will also accept a single-sided flexible disc. However, use of this disc is limited to the IBM format mode of operation.

4-5. TRACKS. There are 77 physical tracks on each side of the disc, with a spacing of 0.0208 inch between tracks (48 tracks per inch). The outermost track is track 0 and the innermost track is track 76.

4-6. RECORDING. Information is stored on the disc as a series of magnetic flux reversals. Since a single head is used to read from and write on each side of the disc, a self-clocking code must be used to store the information.

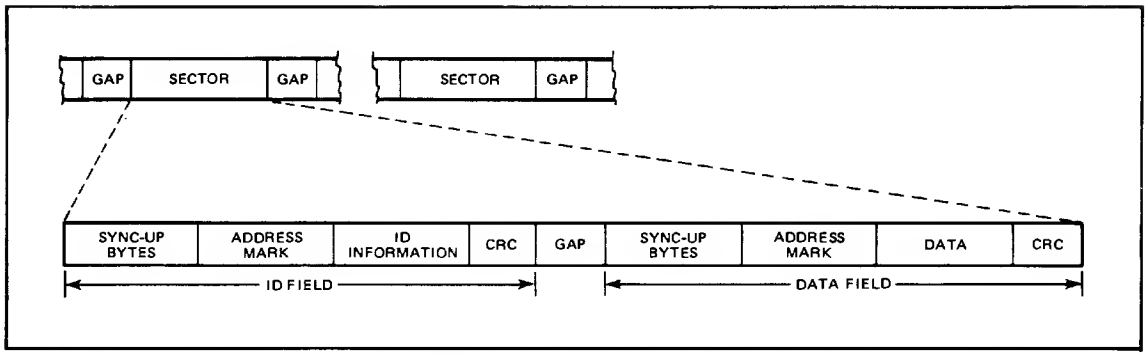
The portion of the disc or the duration of the time used to store a single bit is referred to as a bit cell. The first part of the bit cell is called the clock window and the remainder of the bit cell is called the data window. A flux reversal in the clock window is called a clock transition and a flux reversal in the data window is called a data transition. A bit cell that contains a data transition stores a 1 and a bit cell with no data transition stores a 0.

4-7. TRACK FORMAT. Each track is divided into sectors, as shown in figure 4-1. The data contained in one sector is the smallest amount of information that can be written at a time. The disc is soft-sectored, that is, there is no hardware indication of where each sector starts. Instead, the beginning of each sector is indicated by information recorded on the disc.

In order to allow soft-sectoring, each sector is divided into two fields. First, there is an ID field which contains information to identify the sector. Next, there is a data field which contains the actual data. The ID field is written only when the disc is formatted, never during actual operation. Thus, an ID field serves as a fixed marker for the beginning of each sector. The entire data field is rewritten each time a write operation occurs to the sector.

The makeup of the ID and data fields is similar. Both fields start with a series of sync-up bytes. These bytes end with a long string of identical bits. During a read, the bit string allows the decoder circuitry on the controller PCA time to synchronize itself with the data on the disc. Next comes an address mark byte, which indicates that the beginning of an ID or data field has been found. The data stored in this byte indicates which type of field it is part of. In order that no other byte can be mistaken for an address mark, the address mark byte contains an abnormal pattern of clock transitions. The first bit of an address mark is the opposite type from the last bit of a sync-up field. This feature simplifies detection of address marks.

Following the address marks comes a series of information bytes. In an ID field, these bytes indicate the logical cylinder, head, and sector address of the sector. In a data field, these bytes are the data being stored in the sector.



7310-9

Figure 4-1. Track Format

At the end of each field are two cyclic redundancy check (CRC) bytes. These bytes allow the detection of most errors that occur in the storage and recovery of information from the disc.

There are gaps between each field on a track. The gaps allow for variations in disc rotational speed, and time for the hardware to prepare for the next field.

The sectors are logically numbered consecutively. However, the sectors may occur in any physical order around the track. This allows the sectors to be staggered to optimize system performance.

4-8. TRACK NUMBERING. Each track has a physical address as described previously. There is also a logical track address associated with each good track. The logical track address is written in the ID field of each sector on the track. If a flexible disc has no bad tracks, the logical address of a track is the same as the physical address.

A disc with n bad tracks can be made to look like a 77 − n track disc with no bad tracks. To do this, the logical track address stored in the ID field of each sector of every bad track is set to !FF. Tracks of this type are known as invisible tracks. All non-invisible tracks are then sequentially assigned logical track numbers. Logical track 0 is the outermost good track, not necessarily physical track 0.

4-9. FORMAT DIFFERENCES

Table 4-1 summarizes the principle differences between the IBM format and the HP format. Details of these differences are provided in the following paragraphs.

4-10. CODING. The IBM format uses a single-density encoding scheme known as frequency modulation (FM). The rules for FM coding are as follows:

- A 0 bit cell has no data transition.
- A 1 bit cell has a data transition.

Table 4-1. Format Differences

FEATURE	IBM FORMAT	HP FORMAT
Usable physical tracks	0 – 76	0 – 76
Sectors per track	26	30
Sector numbering	1 to 26	0 to 29
Bytes per sector	128	256
Data order	MS byte first MS bit first	LS byte first LS bit first
Coding	FM	M^2FM
Precompensation required	No	Yes
Sync-up bytes	Six bytes of !00	Four bytes of !00 and four bytes of !FF
Address marks	Missing clock transitions	Extra clock transitions
CRC includes Address mark	Yes	No

- Every bit cell has a clock transition.

The minimum distance between transitions is one-half the bit cell, that is, the distance from a clock transition to a data transition.

The HP format uses a double-density encoding scheme known as modified modified frequency modulation (M^2FM). The rules for M^2FM coding are as follows:

- A 0 bit cell has no data transition.

- A 1 bit cell has a data transition.
- A 0 bit cell has a clock transition if there is no transition in the preceding bit cell.
- A 1 bit cell never has a clock transition.

For the same recording density (flux transitions per inch), there are twice as many data transitions in M^2FM coding as in FM coding.

4-11. PRECOMPENSATION. Transitions which are written close together tend to appear shifted apart when they are read back. This effect is known as bit shift. Due to its large bit cell, the IBM format is not affected by bit shift. However, because of the smaller bit cell used in the HP format, bit shift is noticeable. To compensate for bit shift, certain M^2FM transitions are written closer together. This action is called precompensation. The actual precompensation used on a transition is dependent upon the pattern being recorded.

4-12. ADDRESS MARKS. There are four types of IBM format address marks. All are unique in that they include bit cells which contain no clock transition. The IBM address mark byte is included in CRC generation.

NAME	DATA PATTERN	CLOCK PATTERN	WHERE FOUND
Index AM	!FC	!D7	at index hole
ID AM	!FE	!C7	ID field
Data AM	!FB	!C7	data field
Deleted Data AM	!F8	!C7	data field

At the command set level, a clear D bit indicates a data AM in the data field and a set D bit indicates a deleted data AM in the data field.

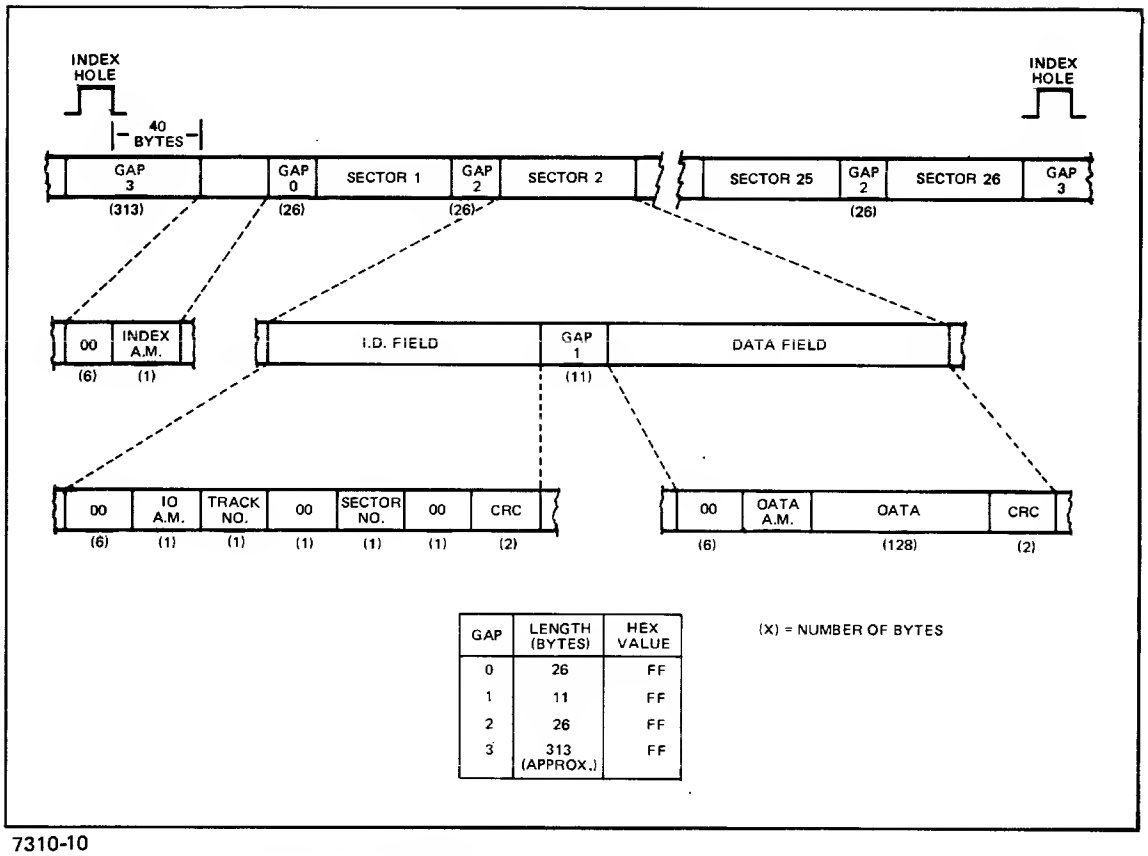
There are four types of HP address marks. All are unique in that they include a bit cell with an extra clock transition. The HP address mark byte is not included in CRC generation.

NAME	DATA PATTERN	CLOCK PATTERN	WHERE FOUND
ID AM	!70	!0E	ID field
Defective Track AM	!F0	!0E	ID field
Data AM	!50	!0E	data field
ECC data AM	!D0	!0E	data field

At the command set level, a clear D bit indicates an ID AM in the ID field, and a set D bit indicates a defective track AM in the ID field.

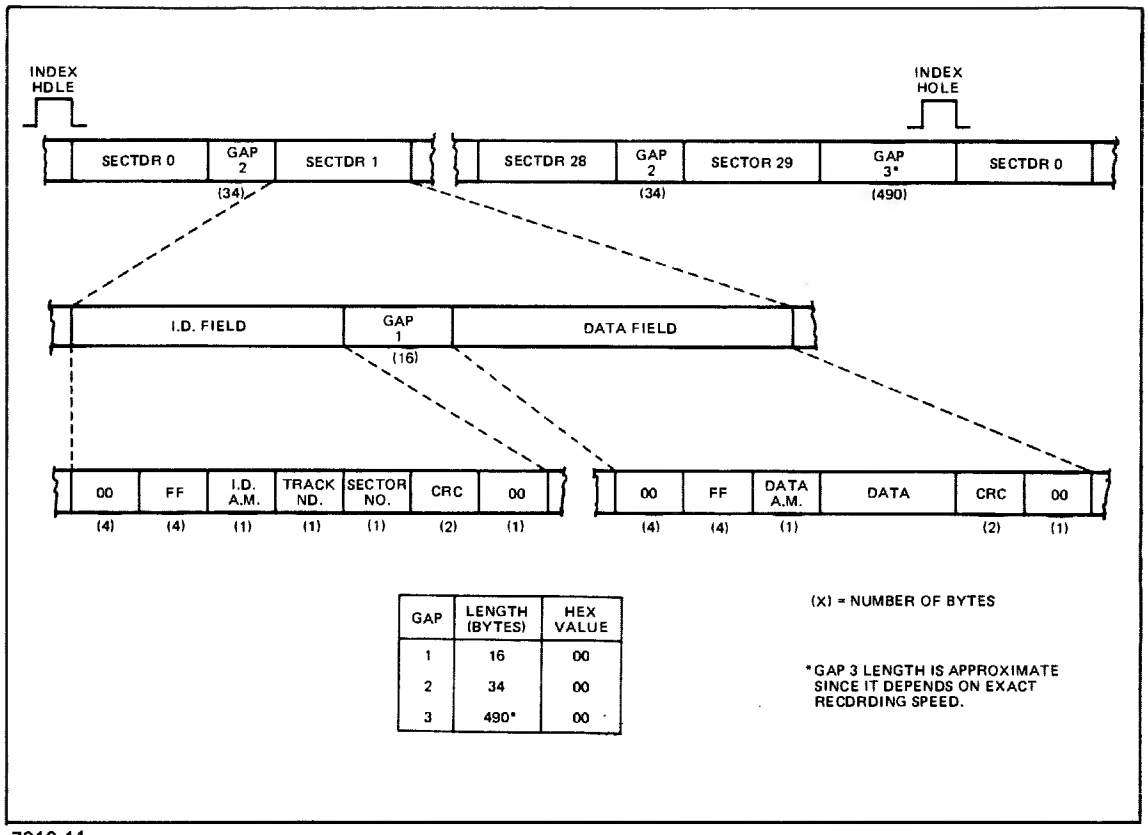
Presently, all data fields contain a data AM. If error correcting code (ECC) bytes are added to the data field in the future, an ECC data AM will be used, allowing interchange between ECC and non-ECC systems.

4-13. TRACK FORMAT. Detailed track formats for the IBM format and HP format are shown in figures 4-2 and 4-3, respectively.



7310-10

Figure 4-2. IBM Standard Sector Recording Format



7310-11

Figure 4-3. Hewlett-Packard Standard Sector Recording Format

4-14. HP 7902 COMMAND SET

4-15. Introduction

The following description of the HP 7902 command set is HP-IB rather than CPU oriented. It is given in terms of operations (mainly bytes sent) over the HP-IB. Since this level is common to any interface to the 7902 it is machine independent.

A basic knowledge of the HP-IB operation including primary commands, secondary commands, and parallel poll operation is assumed.

BUS CONTROLLER -- as used in the manual is the current HP-IB controller in charge of the HP-IB.

CONTROLLER -- the HP 7902 flexible disc controller hardware or firmware.

UNIT -- one of up to four drives connected to the controller.

DISKETTE or DISC -- the coated mylar media used to record data on by the HP 7902.

HP FORMAT -- the double density single or double sided HP standard recording format.

IBM FORMAT -- the single sided IBM standard recording format.

PHYSICAL TRACK NUMBER -- the track number relative to the outer most track on the diskette.

LOGICAL TRACK NUMBER -- the track number recorded on the diskette at a physical track. Logical track numbers may or may not be the same as the physical track number.

HEAD -- one of the two possible heads used to record data in the unit.

TRACK -- the area defined by a cylinder and head address

CYLINDER -- the recording area accessible by the two heads without moving the head actuator.

SECTOR -- the smallest block of data that can be read or written from the disc.

HOST SYSTEM -- the system which contains the BUS CONTROLLER.

4-16. Command compatibility

The HP 7902 belongs to a set of command compatible HP-IB interface discs. All of these discs meet the "HP 300 compatible HP-IB" standards. In addition, the same sequence of HP-IB operations can be used to transfer data to and from any of these discs.

There are two protocols for transferring data and status between the HP 7902 controller and the HP-IB controller, buffered or unbuffered. For compatibility the 7902 supports both modes, nowever the buffered mode is more efficient in terms of HP-IB performance and thus is the preferred mode.

Since the capacity and organization of a floppy disc is different from other HP-IB compatible discs, the allowable range of certain parameters is also different than the other discs.

Certain commands used in formatting a floppy disc or for diagnostic purposes are unique to the 7902. Similarly, certain commands supported by other discs are not supported by the 7902. An unrecognized command causes an error to be set, but has no detrimental effect on controller operation.

4-17. Command sequences

Much of the 7902 command set shown is Section IV is made up from two basic types of HP-IB sequences.

To send information (commands or data) to the 7902, the Bus Controller addresses the 7902 to Listen, and then sends a secondary command byte followed by a series of information bytes. The last information byte sent must be tagged with an EOI. Finally the Bus Controller sends an Unlisten command, and the sequence is complete.

To receive information (status or data) from the 7902, the Bus Controller addresses the 7902 to Talk, and then sends a secondary command byte. At this point the device sends back a series of information bytes (those marked in paragraph 4-24). In some cases the last information byte will be tagged with an EOI. In cases where the last information byte is not tagged with an EOI, an additional byte tagged with an EOI is made available. The extra byte may be used to detect that a byte was dropped on the HP-IB, or it can be used to determine the end of a transfer without maintaining a byte count. Finally the Bus Controller issues an Untalk and the sequence is complete.

Sequences other than the ones shown may in some cases work, but, there is no guarantee that they will be compatible with other HP-IB discs, or with future HP 7902's.

4-18. Parallel poll response

Parallel poll is used as an additional means of communication between the 7902 and the Bus Controller. If the 7902 is ready to accept the next part of a command sequence it will respond to the parallel poll conducted by the Bus Controller.

After accepting most secondary command bytes the 7902 disables the Parallel poll response. This indicates that the device is busy processing the current part of the command sequence. The actual disabling of Parallel Poll response may occur up to 100 microseconds after the secondary is accepted by the 7902. Thus, if the 7902 has Parallel Poll enabled, and the Bus Controller is fast enough to send a command sequence and then conduct a Parallel Poll before the 7902 has disabled the Poll the Bus Controller would see the wrong Parallel Poll response. To solve this problem an intentional delay can be introduced, or a DSJ command (this disables Parallel Poll) can be issued before other commands.

The use of the DSJ command as a Parallel Poll response interlock does not apply in two cases. First, a DSJ cannot be used to disable the poll response which occurs in the middle of certain data transfer command sequences. (For example, the buffered write and initialize commands, the transfer of data bytes normally provides an interlock.) However, if fewer than 8 data bytes (the size of our inbound HP-IB FIFO) are written, the Bus Controller should wait 35 microseconds between sending the data and looking for the 7902's Parallel Poll response.

The second exception to the Parallel Poll response interlock concerns the Clear commands. The DSJ command, unlike the Clear commands, may not be a valid or recognized command in all states of the controller. Thus, the controller may reject or not even see the DSJ command and not disable the Parallel Poll response. If the Bus Controller had expected the DSJ to lower the Parallel Poll in the case where the controller can not accept the DSJ the Bus Controller would see the wrong Parallel Poll after the Clear command.

4-19. Track Numbering

Starting from the outer track, tracks are numbered sequentially from 0 to 76. These numbers are the PHYSICAL track address. There is also a LOGICAL track address associated with all good tracks. If a disc has no bad tracks, the logical address of a track is the same as the physical address.

A diskette with bad tracks can be made to look like a slightly smaller disc with no bad tracks. To do this, the bad tracks are specially marked to indicate that they have no logical address. A track marked in this way is referred to as an invisible track. The remaining good tracks are sequentially assigned logical track

numbers. Logical track 0 is the outermost good track (it may or may not be physical track 0).

During normal operations the user need be concerned only with logical addresses. The 7902 controller will take care of finding the proper physical address.

4-20. Target Addressing

Each unit has a TARGET address associated with it. This is the logical address of the next sector which will be accessed by a data transfer command or return for an address request. This sector is referred to as the target sector. It is uniquely determined by a target CYLINDER address, a target HEAD address, and a target SECTOR address.

Following a power up or a clear command the target address will be set to cylinder 0, head 0, sector 0.

A seek command sets the target address to the cylinder, head, and sector indicated in the command sequence.

During a data transfer the target address is automatically updated so the successive logical sectors can be read without issuing a seek to each sector. This includes updates which cross track or cylinder bounds. The HP 7902 is always in cylinder mode, that is, the head address will be incremented before the cylinder address.

If a data transfer terminates abnormally, the target address is left pointing at the sector which caused the termination.

4-21. The D Bit

Each sector has a flag called the D Bit. It is used to indicate that a track is defective (which is different than invisible). The D Bit can be set or cleared using the initialize command. A set D Bit affects the read, write and format commands and is indicated in the returned status.

The format command is used to convert all tracks flagged with the D Bit into invisible tracks.

4-22. HP and IBM Formats

The HP-7902 can work with diskettes which use either the HP single or double sided formats or the single sided IBM format. After a disc is inserted in a unit, the first status request for that unit will cause the controller to determine which format is present. This information is available as part of the returned status.

Many details of operation vary slightly for the two formats. These include the allowable range of target address, the updating of target addresses, and the effect of the D Bit. These dif-

ferences will be noted in the appropriate command descriptions.

4-23. Holdoffs

The HP 7902 will not execute most operations when it enters either of the two states described below. It is very important to know these states and the commands that will remove the holdoffs.

1) DSJ = 2 or Power on State

This state is entered after:
a. the 7902 is powered up
b. after the execution of the initiate self test

As long as DSJ=2, a value unique to this state, the commands listed below will not be executed. There are however three commands which may be executed either to change the DSJ or override its holdoff. These commands are:

a. the DSJ command,
b. the CLEAR commands,
c. the COLD LOAD READ command.

For both DSJ and Clear the DSJ value becomes 0, the LOAD READ will override the holdoff and set the DSJ according to the outcome of the read.

The only way for the Bus Controller to realize that the device was in the power on state is by sending the DSJ command (which clears the state).

The purpose of this holdoff state is to withhold all operations that may occur during the normal 7902 usage until the Bus Controller can become aware that the power has been restored.

The following is a list of the commands not executed while in the DSJ=2 state:

a. all Read commands
b. all Write commands
c. Verify
d. Initialize
e. Format
f. Seek
g. End
h. Request status
i. Request disc address commmands

The 7902 will, however, respond to a TALK command from the above group by sending one byte (of value 1) tagged with an EOI. Also, all data bytes sent to the 7902 as part of the commands listed above will be accepted but ignored. These

actions will cause the 7902 not to hang (timeout) the HP-IB until the Bus Controller is aware of the holdoff.

2) First Status State

This state is entered for a particular drive after:

a. a diskette is inserted in the drive during normal operation,
b. the 7902 is powered up with a disc in the drive,
c. the 7902 is issued a initiate self test command, with a diskette in the drive.

When this state is entered, bit 12 of the Status 2 word for the drive(s) affected is set. All operations requiring access to the newly inserted disc are disabled until the status of the drive is requested or the Cold Load Read command is issued.

The holdoff ensures that the HPIB controller is aware that the diskette is a newly inserted one before it is actually accessed. In addition, the first request of status for that drive will cause the device to find out the format of the newly inserted diskette, therby enabling proper use of the disc.

Commands not executed while First Status is set are:

a. read commands
b. write commands
c. Verify
d. Initialize
e. Format
f. Seek

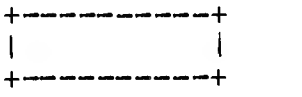
It should be noted that after a power on has occurred for the 7902 or after the execution of the Initiate Self command, the DSJ is set to 2 and the First Status bit is set for any drive containing a disc. Thus, both holdoffs, DSJ and First Status, will be in effect.

Therefore, to enable access to a disc, two command sequences may be used. They are:

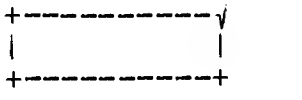
a. a DSJ or Clear followed by a Status command
b. a Cold Load Read command

4-24. COMMANDS

The details of the HP 7902 HP-IB command set are given in this section. The following conventions are used:



Byte sent from the Bus Controller to the 7902.



Byte sent from the 7902 to the Bus Controller.

P
P
D

Parallel Poll disabled

P
P
E

Parallel Poll enabled

ADDR — The 7902's current HP-IB device address

P — HP-IB parity bit

UUUU — Unit number (0<=UUUU<=3)

S1 — Status one

S2 — Status two

COMMAND TABLE

	T/L	Secondary	Opcode	#Bytes
IDENTIFY	T	ADDRS	---	-
DSJ	T	!10	---	1
READ SELF TEST	T	!1F	---	2
READ LOOP BACK	T	!1E	---	1/256
REQUEST STATUS	L	!08	!03	2
REQUEST STATUS	L	!0A	!03	2
REQ LOGICAL ADDRESS	L	!0A	!14	2
REQ LOGICAL ADDRESS	L	!0B	!14	2
REQ PHYSICAL ADDRESS	L	!0C	!14	2
SEND STATUS OR ADDRESS	T	!08	---	4
UNIVERSAL CLEAR	U	---	---	-
SELECTED DEVICE CLEAR	L	---	---	-
HP 300 CLEAR	L	!10	---	1
INITIATE SELF TEST	L	!1F	---	2
WRITE LOOP BACK	L	!1E	---	1/256
DOWN LOAD CONTROLLER	L	!0F	---	1/256
DOOR LOCK	L	!0C	!19	2
DOOR UNLOCK	L	!0C	!1A	2
HP-IB CRC	T/L	!11	---	-
SEEK	L	!08	!02	6
END	L	!08	!15	2
BUFFERED READ	L	!0A	!05	2
UNBUFFERED READ	L	!08	!05	2
VERIFY	L	!08	!07	4
BUFFERED READ VERIFY	L	!0B	!05	2
UNBUFFERED READ VERIFY	L	!0C	!05	2
COLD LOAD READ	L	!08	!00	2
ID TRIGGERED READ	L	!0B	!06	2
SEND DATA	T	!00	---	-
BUFFERED WRITE	L	!09	!08	2
UNBUFFERED WRITE	L	!08	!08	2
INITIALIZE	L	!08	!0B	2
FORMAT	L	!0C	!16	4
RECEIVE DATA	L	!00	---	-

Command Table:

! - Hexadecimal number
T - Talk Primary
L - Listen Primary
U - Universal Primary

4-25. Sense Commands

4-26. IDENTIFY

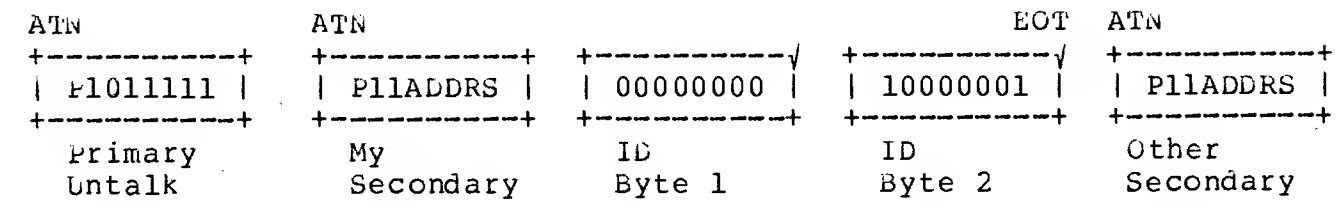
Type: Sense

Purpose: The HP 7902 will return a code unique to the flexible disc subsystem to allow for auto configuration systems.

Description: Upon the reception of a Talk 31 followed by the secondary corresponding to the 7902's current HP-IB address, the 7902's PHI will respond by sending the ID bytes of 0 and 81 Hex, the second byte being tagged with an EOI.

The identify sequence is more fully described in the HP 300 I/O and PHI documentation.

HP-IB Sequence:



4-27. DSJ

Type: Sense

Purpose: The 7902 returns a byte indicating if the last operation completed normally or abnormally, or if the power to the 7902 has just been restored, or if a parity error has been detected on the HP-IB. The DSJ command also provides a way to disable the 7902's Parallel Poll response.

Description: After accepting the DSJ secondary, the 7902 disables its Parallel Poll response (within 100 microseconds) and returns a byte (the DSJ byte) reflecting the status of the controller.

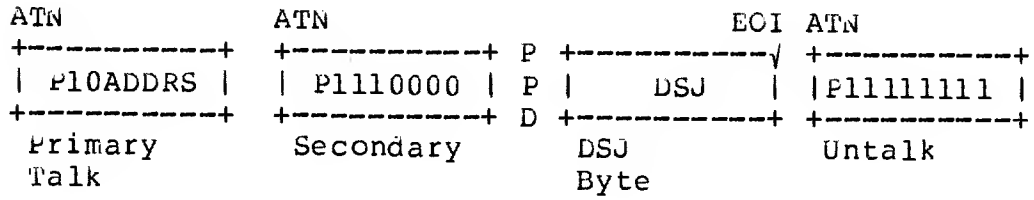
DSJ=0 - The 7902 completed its last operation normally.

DSJ=1 - The 7902 aborted its last operation abnormally. Status will indicate the current error.

DSJ=2 - The 7902 has just completed a power up sequence and is in the DSJ=2 holdoff state.

DSJ=3 - A parity error has occurred on the HP-IB. Repeat the request to receive the pre-parity error DSJ.

HP-IB Sequence:



Status: No errors

S1 - 0
S2 - Unchanged
DSJ - For DSJ=0 or DSJ=1 unchanged
- For DSJ=2 then 0
- For DSJ=3 then last DSJ

Illegal secondary

S1 - I/O program error
S2 - Unchanged
DSJ - 1

Parallel Poll: Parallel Poll is disabled after the reception of the secondary and is not reenabled after the completion of the command.

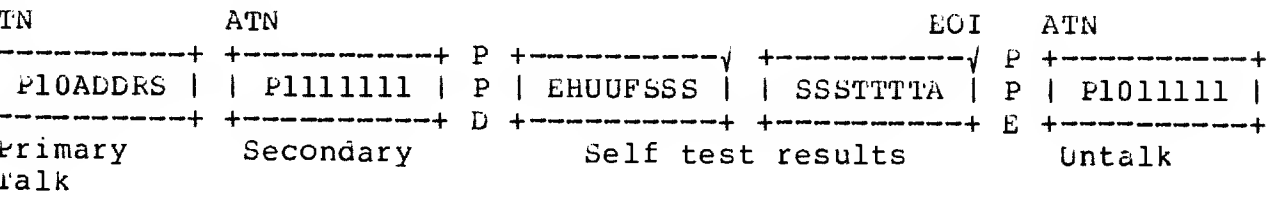
4-28. READ SELF TEST RESULTS

Type: Sense

Purpose: The 7902 returns the results of the last self test the 7902 has performed. This is useful after the initiate self test command or after the 7902 has been powered on (the 7902 performs a self test at power on).

Description: After receiving the self test secondary, the 7902 makes two bytes of the self test results available. The second byte will be tagged with an EOI.

HP-IB Sequence:



where:

E - ERROR BIT. If on then an error has occurred.

H - HEAD NUMBER. Indicates which head the the read or write test failed on.

UU - UNIT NUMBER. Indicates which unit was selected when the error occurred.

F - FORMAT OF OPERATION. Indicates if the controller was in IBM (0) or HP (1) operation at the time of failure.

SSSSSS - SUBTEST NUMBER. Number of the failing subtest.

TTTT - TEST NUMBER. Number of the failing test.

A - '*' LED. Indicates state of the '*' LED.

Status: No errors

S1 - 0
S2 - Unchanged
DSJ - Unchanged

Illegal Secondary

S1 - I/O program error
S2 - Unchanged

Parallel Poll: If less then the specified number cf bytes is accepted by the HP-IB Contoller, the Parallel Poll response is assured to be reenabled upon the reception by the device of the Untalk command.

4-29. READ LOOPBACK RECORD

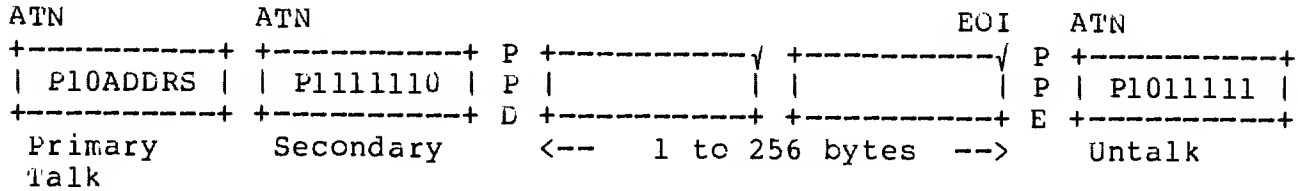
Type: Sense

Purpose: The 7902 sends up to 256 bytes (see WRITE LOOPBACK RECORD) from its internal data buffer over the HP-IB. This is used by diagnostics to test the HP-IB data path.

Description: Upon accepting the Loopback secondary, the 7902 sends the bytes stored in its internal buffer. The most significant byte of the first word is transferred first. The 256th byte will be tagged with an EOI and the transfer terminated. If fewer than 256 bytes are requested, the device will realize that the transfer is complete when:

a. the 7902 has been untalked,
b. it accepts another byte from the HP-IB.

HP-IB Sequence:



Status: No errors

S1 - 0
S2 - Unchanged
DSJ - Unchanged

Illegal secondary

S1 - I/O program error
S2 - Unchanged
DSJ - 1

Parallel Poll: If less then the specified number of bytes is accepted by the HP-IB Contoller, the Parallel Poll response is assured to be reenabled upon the reception by the device of the Untalk command.

4-30. REQUEST STATUS

Type: Sense

Purpose: The device returns four bytes of status information. These status bytes indicate how the last attempted operation completed, which unit was involved, and the current status of the unit specified.

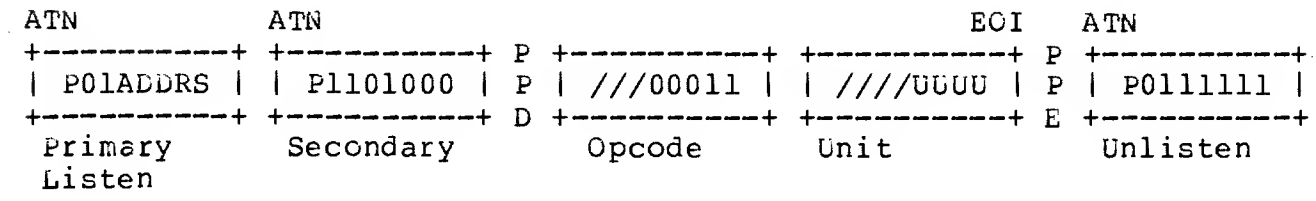
Description: After receiving the request status command, parallel Poll response is disabled. If the unit's first status bit is set, the 7902 attempts to determine the type and format of the current diskette (this may take up to 10 seconds). After the status operation has completed the Parallel Poll response is reenabled.

Note: There is alsc an Unbuffered status request which uses a different secondary.

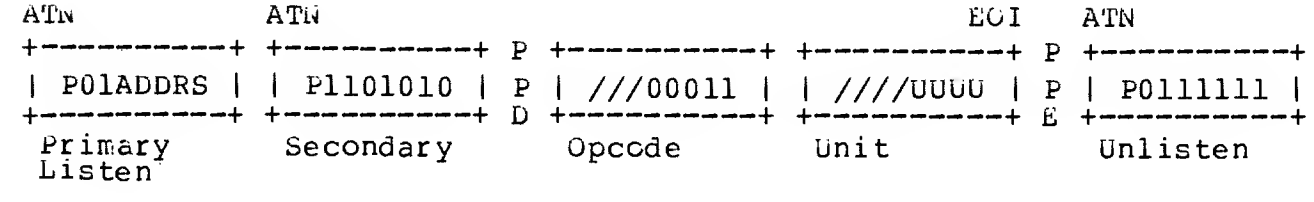
After the Send Status secondary, the 7902 sends four bytes of status information. The first two bytes (known as Status 1) includes information about the last operation which the device performed. The Status 1 (S1) Unit field indicates which drive was involved in the operation. The D Bit is set if a D bit was encountered during the operation.

HP-IB Sequence:

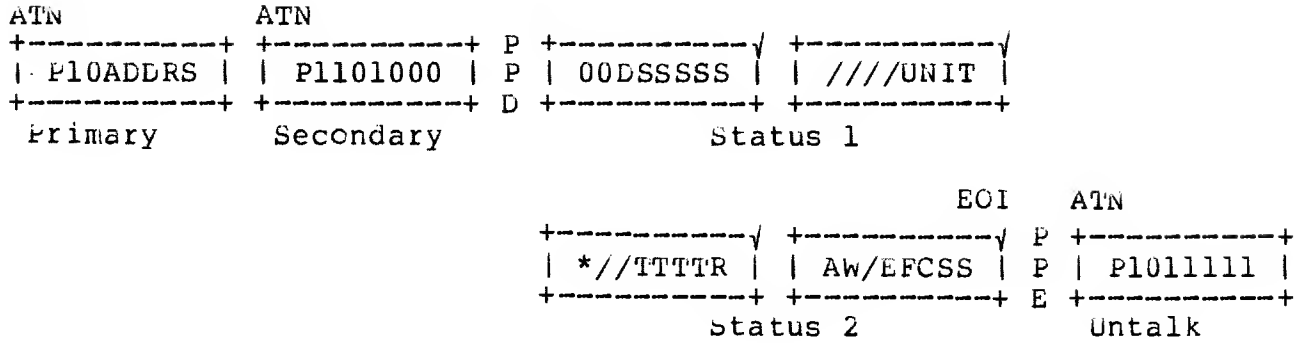
REQUEST STATUS (BUFFERED)



REQUEST STATUS (UNBUFFERED)



RECEIVE STATUS



where:

UNIT		--	Unit number
D		--	D Bit
SSSSS		--	Status 1 (See next page)
*		--	Set if one or more starred bits is set.
TTTT		--	Diskette type
R		--	Reserved
A		--	Drive attention
W		--	Diskette write protected
E	*	--	Drive fault
F		--	First status bit
C	*	--	Seek check
SS	*	--	Drive ready status

Status 1	Meaning
00000	NORMAL COMPLETION. The operations completed without error, or the the controller has just been cleared, or powered up.
00001	ILLEGAL OPCODE. The last command contained an opcode which is not recognized by the 7902.
00111	CYLINDER COMPARE ERROR. The target cylinder was not found.
01000	UNCORRECTABLE DATA ERROR. The disc read or verify operation was terminated because a data error was detected.
01001	SECTOR COMPARE ERROR. The target sector cannot be found in the current track. Up to two passes of the track are made before this status is set.
01010	I/O PROGRAM ERROR. An illegal HP-IB secondary or sequence has been received by the controller. This status can only be set if the previous S1 was zero.
10001	DEFECTIVE TRACK OR SECTOR. During a HP write, read read verify, or verify a set D Bit was encountered.
10010	RETRYABLE HARDWARE ERROR. An internal hardware timing error occurred during a data transfer or seek. The operation should be retried once.
10011	STATUS 2 ERROR. Some condition in Status 2 prevented the drive related operation from completing normally. These conditions include: 1. Specified unit is between 0 and 3 but that drive is not connected to the controller. 2. There is no disc in the drive. 3. A hardware problem is detected in the drive. 4. The disc is unformatted or has an unknown format. 5. The disc is write protected (error only during a disc write operation). 6. The selected drives First Status Bit is set.

10111 UNIT UNAVAILABLE. A command included a request for a unit number less than 0 or greater than 3.

11111 DRIVE ATTENTION. The indicated drive is requesting attention because:

1. A seek completed normally.

2. A seek command failed due to:

   a. Drive fault,
   b. Out of bounds target cylinder or sector,
   c. The controller cannot find the target address.

3. Following an End command, a change in drive status was detected, including:

   a. Inserting a disc
   b. removing a disc
   c. connecting a drive
   d. disconnecting a drive

Status 2	Meaning
*	STATUS 2 ERROR. This bit is set if one or more of the following bits are set in Status 2: a. Drive Fault b. Seek Check c. Any drive Not Ready error
TTTT	DISC TYPE. These four bits indicate the type and format of the disc currently present in the selected drive as follows: 0000 - Empty drive 0001 - Blank or Unknown format single sided 0010 - HP format single sided 0101 - Blank or Unknown format double sided 0110 - HP format double sided 1000 - IBM format single sided
A	ATTENTION. This bit is set when a seek completes (successfully or unsuccessfully), or following an End command when status 2 changes. It is cleared after the status is read.
P	WRITE PROTECTED. The diskette in the selected drive has the write protect notch present.
D	DRIVE FAULT. This bit is set after the following occurs: a. Drive goes not ready after End command, b. Drive goes not ready during data transfer, c. Hardware failure, Drive Fault is cleared after the status is read.
F	FIRST STATUS BIT. This bit is set when a diskette is present in the selected drive after: a. Power on, b. the door is closed, c. Clear commands. First Status is cleared after the status is read.
C	SEEK CHECK. This bit is set when a seek fails for one or more of the following reasons: a. An out of bounds target sector was specified b. An attempt was made to access a non-existent physical track, c. The seek algorithm could not find the target logical track.

The Seek Check bit is cleared after the status is read.

SS — DRIVE (NOT) READY. These two bits indicate the state of the selected drive as follows:

00 -- Drive Ready
01 -- Undefined
10 -- No drive connected to controller
11 -- No disc in drive

Status: No errors

S1 - 0
S2 - Bits 8, 11, 12, and 13 are cleared
DSJ - 0

Illegal secondary
Illegal command length
Illegal command opcode

S1 - I/O program error
S2 - Unchanged
DSJ - 1

Parallel Poll: If less then the specified number of bytes is accepted by the HP-IB Contoller, the Parallel Poll response is assured to be reenabled upon the reception by the device of the Untalk command.

An extra byte (the value of 1) tagged with an EOI will be sent if the controller requests more than the specified number of bytes. However, this request is not necessary for normal operations.

4-31. REQUEST (Logical) DISC ADDRESS

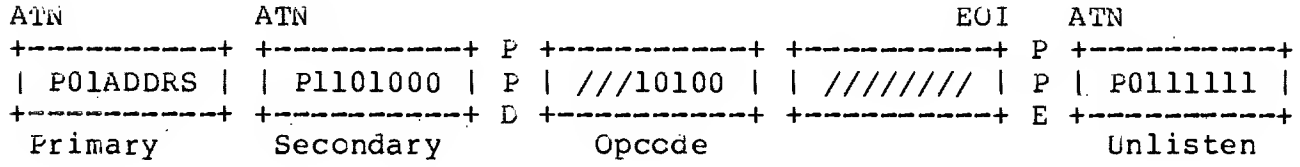
Type: Sense

Purpose: The 7902 returns bytes indicating the current target address. This command is used to determine the address of the offending sector after a data error has occurred.

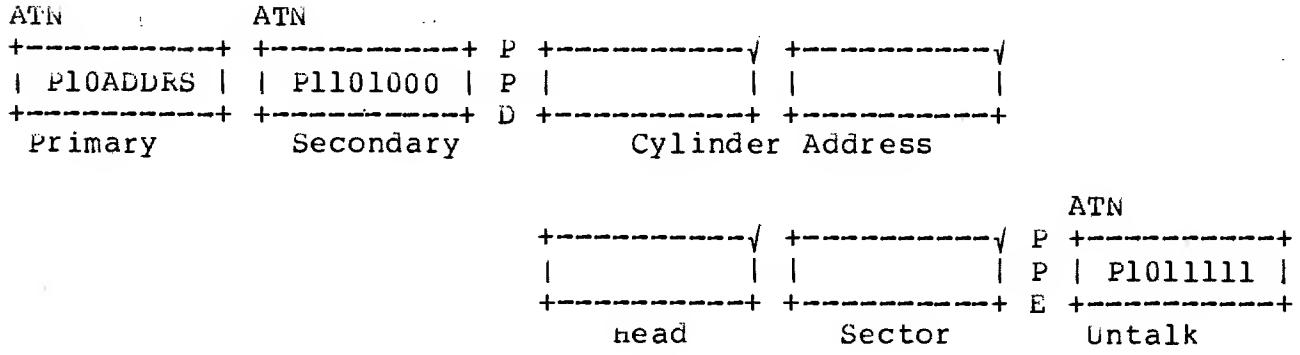
Description: Following reception of the appropriate command sequence the 7902 returns four bytes indicating the current target sector. This includes two bytes of target track address, one byte of target head address, and one byte of target sector address.

HP-IB Sequence:

REQUEST (Logical) DISC ADDRESS



SEND ADDRESS COMMAND



Status: No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Illegal secondary
Illegal command sequence byte count

S1 - I/O Program error
S2 - Unchanged
DSJ - 1

Illegal opcode

S1 - Illegal opcode
S2 - Unchanged
DSJ - 1

DSJ - 1

Parallel Poll: If less then the specified number of bytes is accepted by the HP-IB Contoller, the Parallel Poll response is assured to be reenabled upon the reception by the device of the Untalk command.

An extra byte (the value of 1) tagged with an EOI will be sent if the controller requests more than the specified number of bytes. However, this request is not necessary for normal operations.

4-32. REQUEST (Physical) DISC ADDRESS

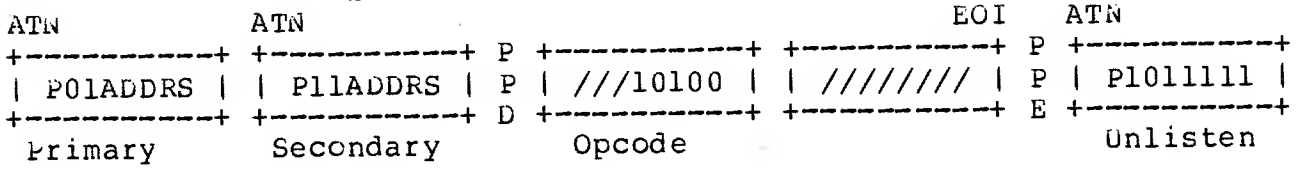
Type: Sense

Purpose: The 7902 returns bytes indicating the physical track on which the head actuator is positioned. This is useful for calculating the number of invisible tracks between the outer most track and the current track. This is done by subtracting the physical track address from the target track address.

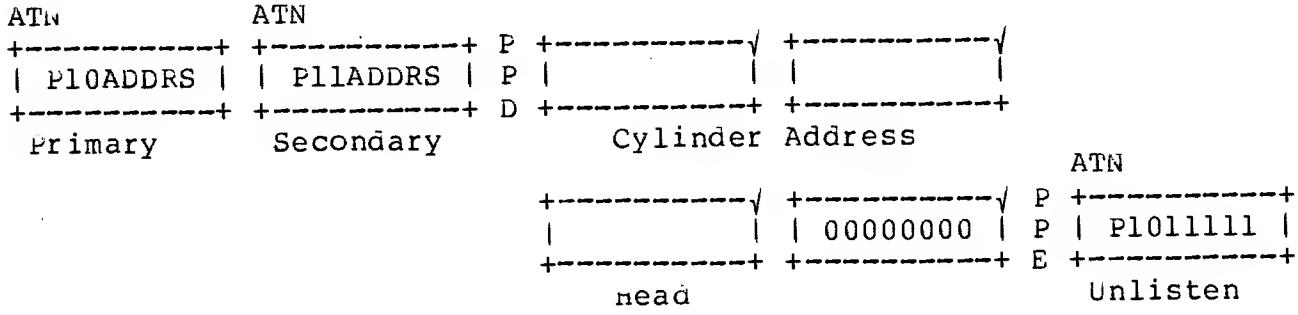
Description: After receiving the request physical command, the 7902 returns two bytes containing the physical cylinder address, one byte containing the head address and one byte of zeros.

HP-IB Sequence:

REQUEST PHYSICAL ADDRESS



SEND ADDRESS



Status: (See Request Logical Address)

Parallel Poll: (See Request Logical Address)

4-33. Control Commands

4-34. UNIVERSAL OR SELECTED DEVICE CLEAR

Type: Control

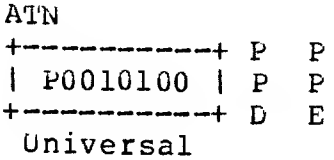
Purpose: A clear places the 7902 in a known state. Thus it is useful when initializing a system on power up or after a host system crash. The clear also allows a power up DSJ of 2 to be cleared by sending a single byte. Since a clear updates the device's HP-IB address, it is useful if the system is being re-configured.

Description: Upon reception of either a universal or selected device clear command, the 7902 stops handshaking with the HP-IB, parallel poll response is disabled and the following are performed:

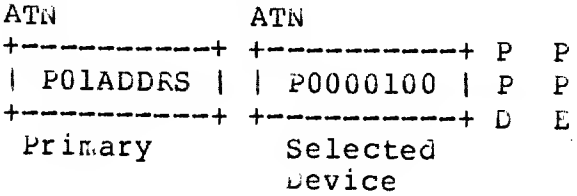
a. the PHI is reset,
b. HP-IB is updated from the device address on the controller board,
c. Status 1 is cleared,
d. Status 2 is updated appropriately,
e. DSJ set to 0,
f. all drives are recalibrated to physical track 0,
g. the Target address is set to cylinder 0, head 0, sector 0,
h. Disable HP-IB parity checking.

HP-IB Sequence:

UNIVERSAL DEVICE CLEAR



SELECTED DEVICE CLEAR



Status: No errors

S1 - 0
S2 - All bits cleared, then bits 11, 14 and 15 are set if appropriate.
DSJ - 0

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

4-35. HP 300 CLEAR

Type: Control

Purpose: This command gives the user the capability to place the 7902 controller in a known state, and, to programatically enable or disable the HP-IB parity check logic.

Description: After reception of the HP-300 clear secondary, the data byte, and the device clear, the contoller sets or clears the HP-IB parity enable in the PHI. See HP 300 I/O ERS for information of parity checking for HP 300 devices.

HP-IB Sequence:

HP 300 DEVICE CLEAR

ATN	ATN	P	EOI	ATN	P	ATN
P01ADDRS	P1110000	P	///////X	P0000100	P	P0111111
		D			E	
Primary Listen	Secondary Device Clear		Control Byte	Selected Device Clear		Unlisten

where: X - HP-IB parity check bit:

0 - Disable parity check,
1 - Enable parity check.

Status: No errors

S1 - 0
S2 - All bits cleared, then 11, 14, and 15 set if appropriate.
DSJ - 0

Illegal secondary
No data byte
Data not tagged with EOI

S1 - I/O Program error
S2 - Unchanged
DSJ - 1

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

4-36. INITIATE SELF TEST

Type: Control

Purpose: This command gives the user the capability to remotely initiate the 7902 self test. The self test results may then be read back using the Read Self Test Results command. Self test takes approx. 7 seconds to complete.

Description: Two bytes are sent following the self test secondary and contain the following information:

The first byte contains the cylinder to be tested and is only pertinent if the W bit is set in the second byte of the command. The W bit is interpreted as follows:

0 -- No write/read test performed,

1 -- The write/read test is performed on the designated cylinder.

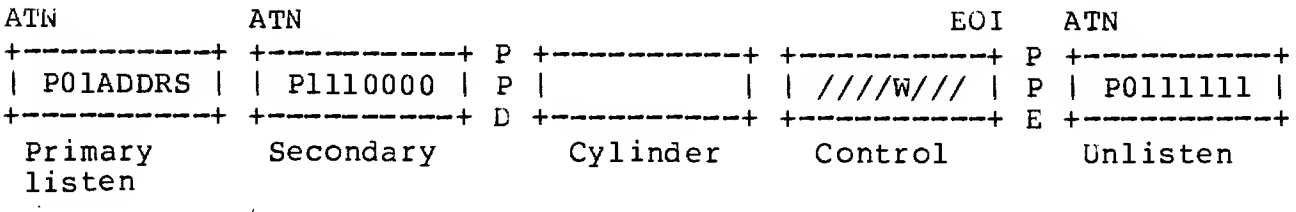
If the write/read test is selected, a double sided diskette is required and all data on both sides of the selected cylinder will be lost.

After the execution of the self test the controller will be in the same state as a power on condition would leave it.

Note: The self test write test will reformat the selected test cylinder. This reformatting will destroy data on the selected cylinder and change the sector interleave and offset so that it may no longer be optimal for the host system. After the write test is performed, the diskette should be reformatted by the Format command.

HP-IB Sequence:

INITIATE SELF TEST



Status: No errors

S1 - 0
S2 - Cleared, the bits 11, 12, 14, and 15 set if appropriate.
DSJ - 2

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

4-37. WRITE LOOPBACK RECORD

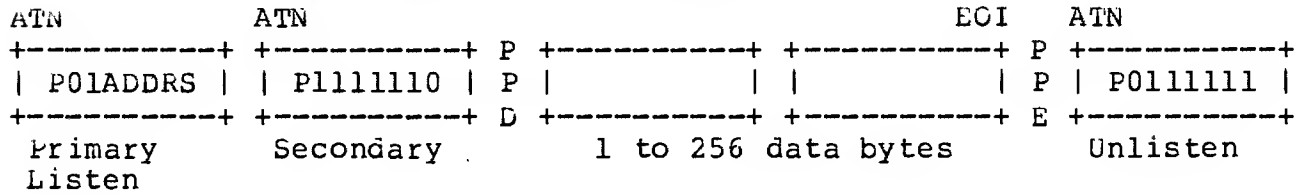
Type: Control

Purpose: The 7902 stores up to 256 bytes in its internal buffer. A diagnostic could use the command, along with the Read Loopback Record, to test the operation of the HP-IB link.

Description: After receiving the Write Loopback Record secondary the controller will store up to 256 bytes in the internal buffers. If less then 256 bytes are sent, the last byte must be tagged with an EOI.

HP-IB Sequence:

WRITE LOOPBACK RECORD



Status: No errors

S1 - Unchanged
S2 - Unchanged
DSJ - Unchanged

Parallel Poll: If less then the specified number of bytes is accepted by the HP-IB Contoller, the Parallel Poll response is assured to be reenabled upon the reception by the device of the Untalk command.

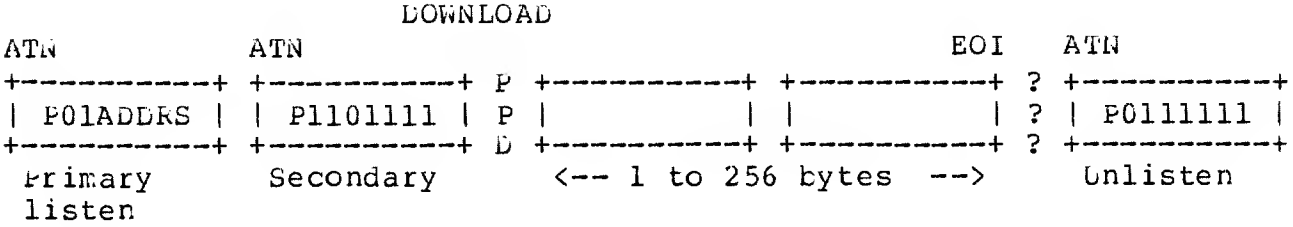
4-38. DOWNLOAD

Type: Control

Purpose: This command allows the downloading and execution of MCC code into the controllers internal RAM memory. It is intended for diagnostic purposes only, and as such should be used with care.

Description: After receiving the Download secondary, up to 256 bytes are stored in the controllers memory starting at location (hex) 56. These bytes are packed two to a word, the odd numbered bytes in the LSB and even numbered bytes in the MSB. Following the reception of the last byte the controller will transfer execution to the downloaded code starting at (hex) 56. Good luck!

HP-IB Sequence:



Note: Updating of status and the operation of Parallel Poll is dependent upon downloaded code.

4-39. SEEK

Type: Control

Purpose: The Seek command updates a units target address and moves the head actuator to the new target cylinder. A seek usually precedes a data transfer operation or a series of consecutive data transfers.

It is important to note that the 7902 controller is totally dedicated to the selected drive during any drive related operation (i.e., the Seek command). This disallows any overlapped seek operation between multiple drives.

Description: The device receives 6 bytes, including the seek opcode, the unit number, and the target cylinder, head and sector address. Checks are made to assure that the specified drive is available, that the entire command has been received, and that the new target address lies within the following bounds:

	HP		IBM
	Single	Double	Single
Cylinder Address:	0<=C<=76	0<=C<=76	0<=C<=76
Head Address:	H=0	0<=H<=1	H=0
Sector Address:	0<=S<=29	0<=S<=29	1<=S<=26

If any of these test fail, the status is updated and the seek command is aborted.

The following algorithim is used to locate a logical target track during the seek operation:

a. Read current cylinder location from disc,

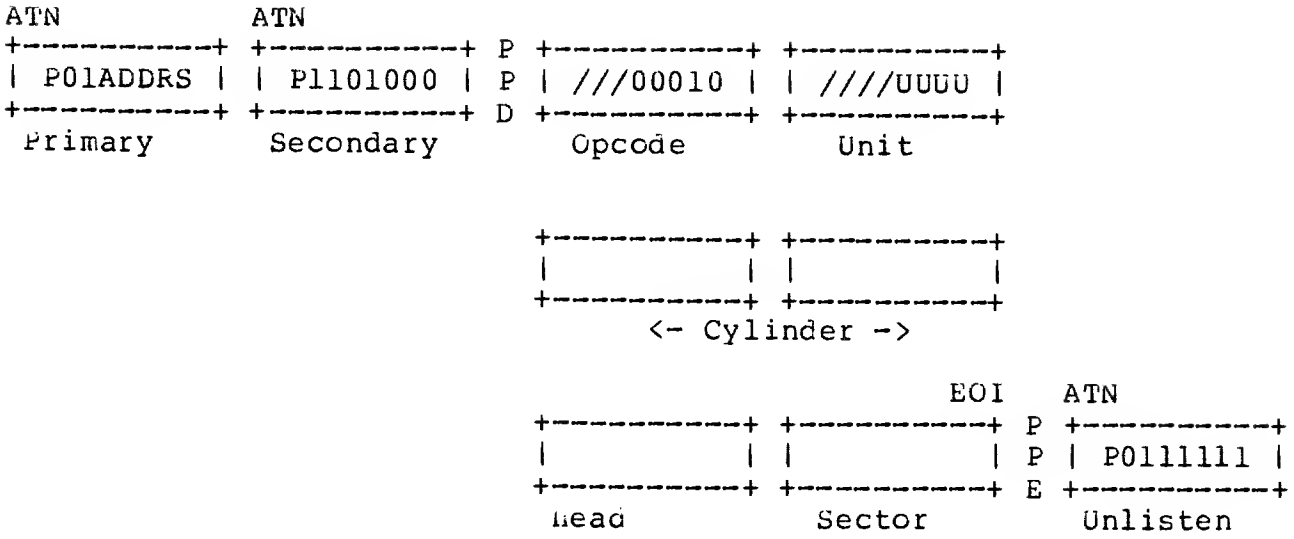
b. If current address is not the location expected then do phyical seek to cylinder 0,

c. Estimate the direction and number of steps to the target cylinder,

d. Step actuator to target, and read current head postion,

e. If not at target cylinder address, repeat steps (c) and (d) until target found or retry exhausted.

HP-IB Sequence:



Status: Successful Seek

S1 - Drive Attention
S2 - Bit 8 set (Drive Attention)
DSJ - 0

Unsuccessful Seek

a. Illegal seek parameter,
Target track not found,
Off end of disc.

S1 - Drive Attention
S2 - Bits 8 and 13 set (Seek check)
DSJ - 1

b. Drive not ready during seek,
Track 0 indicator not found when expected.

S1 - Drive Attention
S2 - Bits 8 and 11 set (Drive fault)
DSJ - 1

Illegal command length

S1 - I/O Program Error
S2 - Unchanged
DSJ - 1

Illegal unit specification

S1 - Unit Unavailable
S2 - Unchanged
DSJ - 1

DSJ = 2 Holdoff

S1 - Unchanged
S2 - Unchanged
DSJ - 2

No diskette or not ready
1st Status Bit holdoff
Disc not formatted or of unknown format

S1 - Status 2 Error
S2 - Unchanged
DSJ - 1

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally. Normal completed is when the target cylinder is reached.

4-40. END

Type: Control

Purpose: The End command serves a dual purpose as follows:

a. It causes the 7902 to cease responding to a Parallel Poll and put the controller and drives in a "stand by" state, and,

b. In case of a status change in any of the drives the 7902 immediately reactivates its Parallel Poll response which can serve as a pseudo interrupt facility to the Bus Controller.

Description: The End command should be issued after a series of commands to a single unit have been completed. The following is performed by the 7902 upon reception of an End command:

a. S1 - 0
S2 - Unchanged
DSJ - 0

b. Disable Parallel Poll response.

c. Wait for change in drive status.

The 7902 will continue to check the status of all drives and will, at the same time, remain ready to execute any new HP-IB command. However, if no new command has been issued to the 7902, and the state of a drive changes since the last time status was requested, the following is performed by the device:

a. Diskette removed

S1 - Drive Attention
S2 - Bits 8 and 11 set (Drive Fault)
DSJ - 1

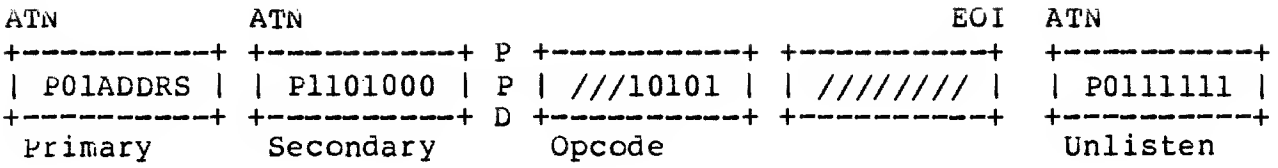
b. Diskette inserted

S1 - Drive Attention
S2 - Bits 8 and 12 set (First Status)

c. Parallel Poll is enabled on the HP-IB

HP-IB Sequence:

END COMMAND



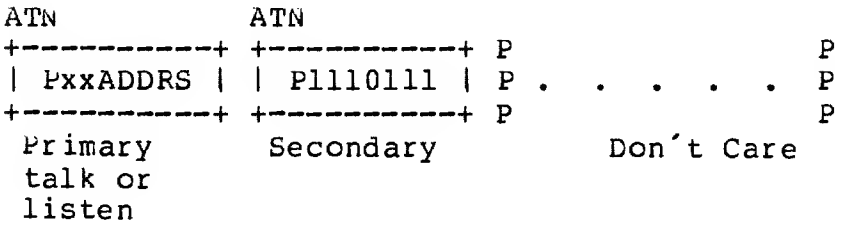
4-41. HP-IB CRC SECONDARY

Type: Control

Purpose: The HP-IB CRC Secondary is part of the 7902 command set to be compatible with future HP-IB devices who use the CRC data tests of the future PHIs. The 7902 will ignore this command, that is, not set I/O Program error when it is received.

Description: The 7902 can be addressed to talk or listen. If addressed to listen any number of data bytes may be sent, if addressed to talk an EOI will be sent over the HP-IB.

HP-IB Sequence:



Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

4-42. DOOR LOCK

Type: Control

Purpose: This command will lock the diskette access door on the selected drive.

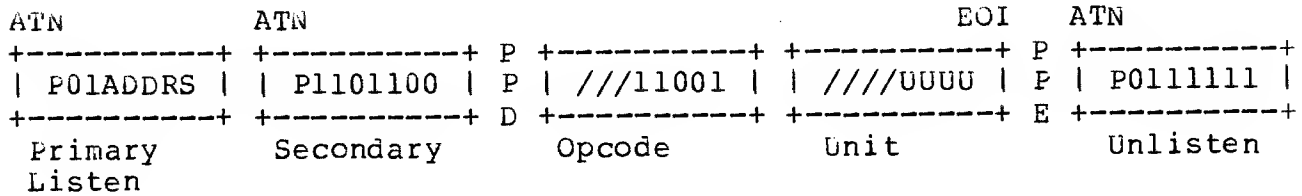
Note: Normal operation of the 7902 will lock the access door whenever a drive is selected for an operation. Special hardware in each drive will keep the drive selected (and door locked) for about 1 to 2 seconds after the command has completed.

Description: After sending the secondary, the opcode and the unit number, the 7902 will issue a command to the selected drive to lock the door. The door will remain locked until one of the following conditions:

a. a Door Unlock command,
b. a Clear command,
c. an Initiate Self Test command,
d. a System Reset signal to the controller backplane.

HP-IB Sequence:

DOOR LOCK REQUEST



Status: No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Illegal secondary
Illegal Opcode
Not 2 data bytes in command

S1 - Error Number
S2 - Bits 8, 11 and 13 set if appropriate
DSJ - 1

4-43. DOOR UNLOCK

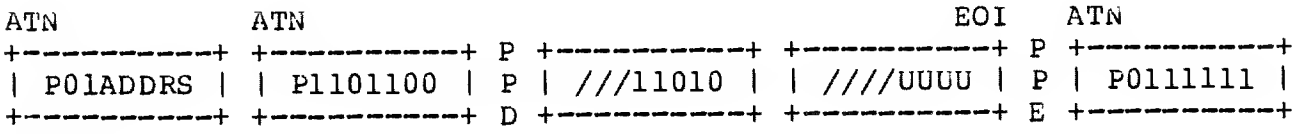
Type: Control

Purpose: This command is used to unlock the diskette access door. It is useful after the Door Lock command is given. (See Door Lock)

Description: After the reception of the secondary, opcode, and unit number the 7902 will issue a command to the selected drive to unlock the access door. This command has no effect if the door was not previously locked.

HP-IB Sequence:

DOOR UNLOCK



Listen Status: (See Door Lock)

4-44. DISC READ COMMANDS

4-45. BUFFERED READ

Type: Disc Read

Purpose: Data is transferred through an internal buffer in 7902 before being sent to the HP-IB. This allows HP-IB data transfers to be asynchronous with the disc, and to vary from an arbitrarily low rate to about 137 Kbytes per second. The maximum number of bytes to be transferred in a buffered read is 1 sector, the read request must be repeated for each additional sector transferred.

Description: Following reception of the read command, Parallel Poll response is disabled, and the status of the specified unit is checked. If the Unit can be accessed, then the current track number is read and compared with the target track address. If they differ, a seek to the target track is performed. This may occur if the actuator has slipped, or if an auto-increment to the the next track is required.

If a HP format disc is being used, then the target sector's 256 bytes are read into the controllers buffer. If the read completes sucessfully, then target address is incremented by one sector. If the sector is not found, a CRC error is indicated, or if a D Bit is encountered, the target address is not incremented.

If an IBM disc is present, then the target sector's 128 bytes are read into the controllers buffer. If the read completes sucessfully, then the target address is incremented by one. If the target sector is not found, a CRC error is indicated, or the D Bit is encountered, the target address is not incremented.

After the data has been buffered into the controller the Parallel Poll response is reenabled, indicating that the device has data ready to transmit. The Bus Controller should request the data by issuing the 'Send Data' secondary. Upon receiving the secondary the 7902 again disables Parallel Poll.

If the read was terminated before data was loaded into the buffer (i.e., any error except CRC or D Bit on), the device will respond by sending an EOI tagged byte, and enabling Parallel Poll response.

If there was no error, or the a CRC error or D Bit was encountered, the sector's worth of data is made available. The Bus Controller can take any number of bytes up to a sectors length. If more than 1 sector is requested, the 7902 will send a byte tagged with an EOI. The number of bytes taken has no effect on the updating of the target address.

If the D Bit or CRC error occurs, the corresponding data may be invalid.

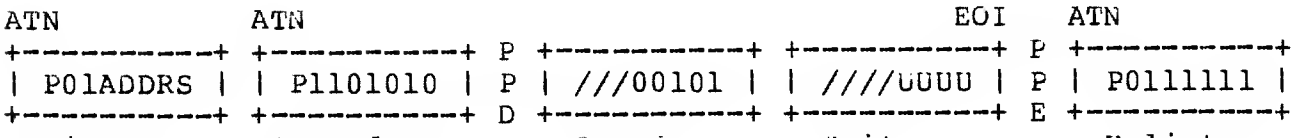
Parallel Poll response will be enabled after sending the last byte, sending another secondary to the 7902 or by untalking the 7902.

If more than 1 sector is to be transferred then, any number of buffered reads can be used in succession. If an error is encountered, all following reads will be held off due to a bad DSJ, so there is no chance of an error in the middle of a long read going unreported. However, error detection will be quickened if:

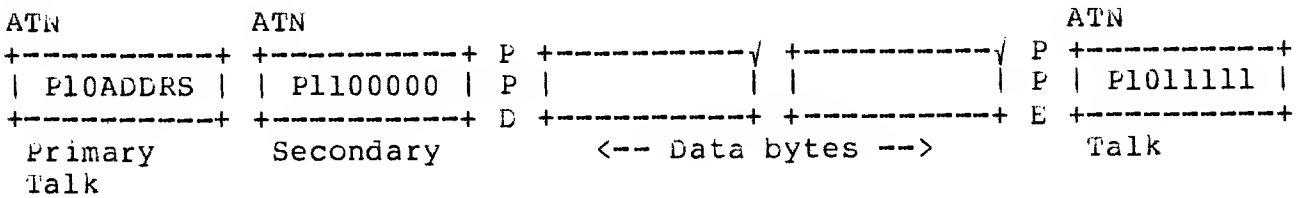
a. a DSJ is used after each read
b. the reception of an EOI to indicate an error

HP-IB Sequence:

BUFFERED READ REQUEST



SEND DATA REQUEST



Status: No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Unsuccessful Read

S1 - Error
S2 - Bits 8, 11 and 13 set if appropriate
DSJ - 1

Requirements for Execution:

a. 2 data bytes received in command
b. Unit 0<=U<=3
c. DSJ <> 2
d. Disc present and ready
e. Not First Status
f. Status 1 = Normal completion,
I/O program error, or
illegal opcode error.

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

If less then the specified number of bytes is accepted by the HP-IB Controller, the Parallel Poll response is assured to be reenabled upon the reception by the device of the Untalk command.

An extra byte (the value of 1) tagged with an EOI will be sent if the controller request more than the specified number of bytes. However, this request is not necessary for normal operations.

4-46. UNBUFFERED READ

Type: Disc Read

Purpose: The Unbuffered Read allows more than 1 sector to be transferred from the disc to the Bus Controller using a single command.

Description: Note: The following description of Unbuffered Read describes a pseudo unbuffered operation. At the time of the writing of this document a true unbuffered read was being designed. If implemented, refer to future revisions of this document for the correct description.

Following reception of the read command, Parallel Poll response is disabled, and the status of the selected unit is checked. If the unit can be accessed (Requirments for Execution) the internal buffer is filled with a sector of data from the disc, just as in the buffered read. Now the 7902 waits for the Send Data command, then begins sending data to the Bus Controller. When all the bytes from the sector have been sent, the 7902 then reads the next sector into the internal buffer and sends it to the Bus Controller. This process is kept up until some termination condition is reached.

If the unit becomes unavailable, or a sector cannot be found when the buffer is empty, or if a CRC error or D Bit is encountered, the sector in the buffer is sent followed by an EOI.

If the unit becomes unavailable, or a sector cannot be found when the buffer is not empty, or if a CRC error or D Bit is encountered, the sector in the buffer is sent followed by a byte tagged with an EOI.

If at any time during the operation, the device notices that it has been untalked, or that the Bus Controller has sent a byte, the transfer is stopped.

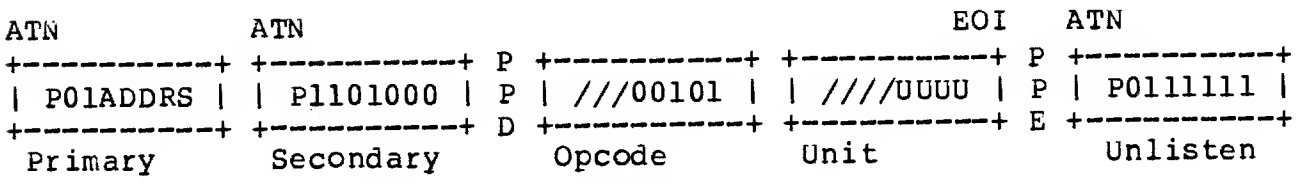
Following any of the above terminations, status is updated, and poll response is reenabled. If there was an error in reading the data from the disc, the target address is left pointing to the sector in which the error occurred. Otherwise, the target address points to the sector following the last sector read from the disc.

As has been seen, the unbuffered read actually uses the internal buffer to store the data. However,

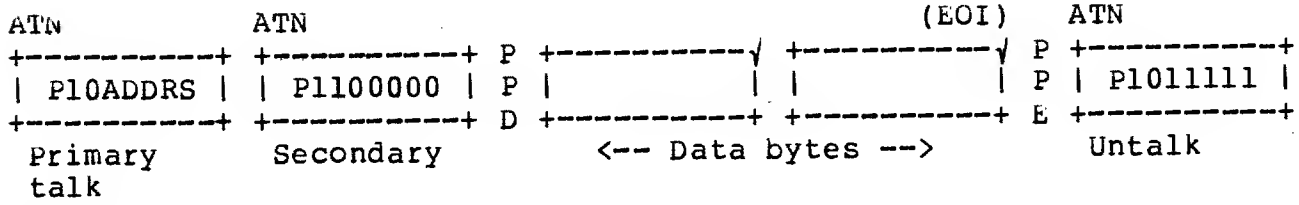
the protocol used is unbuffered in that poll response is not used to indicate when data is available. Thus, there is a pause in data flow to the HP-IB each time the buffer is refilled from the disc. This pause occurs at the beginning of the read, and after every sector has been transferred. Depending on when the read is started and the sector interleaving, this pause may be up to 160 milliseconds long.

HP-IB Sequence:

BUFFERED READ REQUEST



SEND DATA REQUEST



Status:

No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Unsuccessful Read

S1 - Error
S2 - Bits 8, 11 and 13 set if appropriate
DSJ - 1

Requirements for Execution:

a. 2 data bytes in command
b. 0<=UNIT<=3
c. DSJ <> 2
d. Disc present and ready
e. First Status Bit not set
f. Status 1 = Normal completion, I/O program error, or illegal opcode error.
g. Disc not write protected

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

If less then the specified number of bytes is accepted by the HP-IB Contoller, the Parallel Poll response is assured to be reenabled upon the reception by the device of the Untalk command.

4-47. VERIFY

Type: Disc Read

Purpose: The Verify command is a read with reduced margins which does not transfer data to the HP-IB. This is useful for performing a surface analysis of the disc, or, checking the integrity of the data on the disc.

Description: As with other read commands, Parallel Poll is disabled, the availability of the unit is checked, and the target sector is sought. Starting with the target sector, consecutive sectors are read using reduced margins until any of the following occurs:

a. Unable to begin verify operation,

b. Sector count given in the command expires,

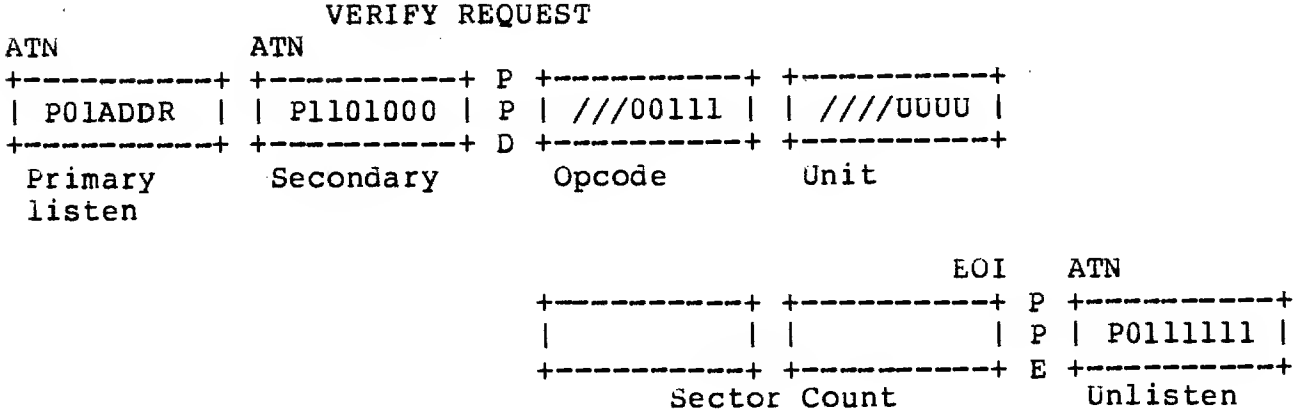
c. A seek or read error occurs,

d. A sector marked defective is detected,

e. The end of the diskette is reached.

Parallel Poll response is reenabled upon completion of the verify. If an error was detected, the target address points to the sector in which the error occurred. Otherwise, the target address points to the sector following the last sector read.

HP-IB Sequence:



Status:

No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Verify error

S1 - Error
S2 - Bits 8, 11 and 13 set if appropriate
DSJ - 1

Requirements for Execution:

a. 4 data bytes in command
b. 0<=Unit<=3
c. DSJ <> 2
d. Disc present and ready
e. Not First Status Bit
f. Sector Count >= 0

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

4-48. BUFFERED READ VERIFY

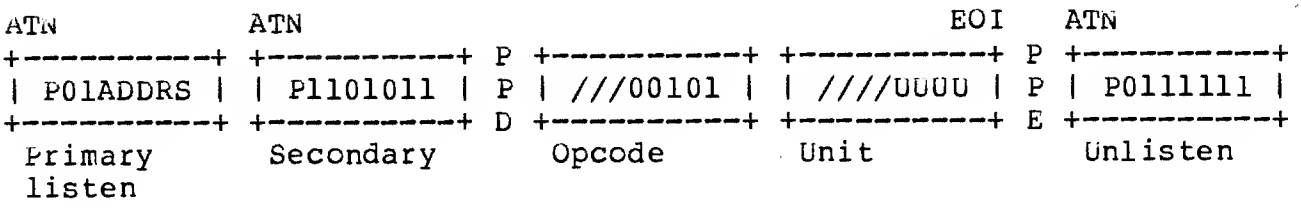
Type: Disc Read

Purpose: The Buffered Read Verify is identical to the buffered read command except that the margins for good data are reduced. This command gives a high confidence that the data on the disc is correct.

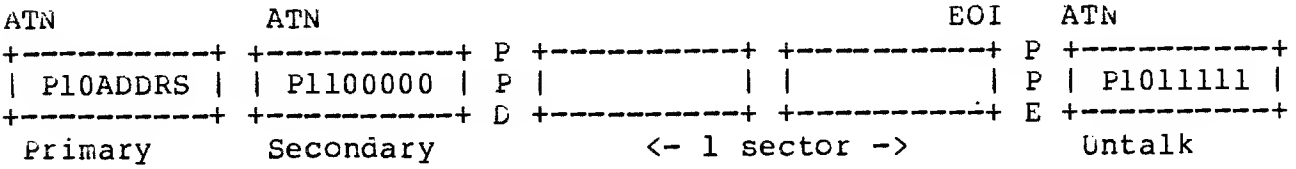
Description: (See Buffered Read)

HP-IB Sequence:

REQUEST BUFFERED READ VERIFY



SEND DATA



Status: (See Buffered Read)

Requirements for Execution: (See Buffered Read)

4-49. UNBUFFERED READ VERIFY

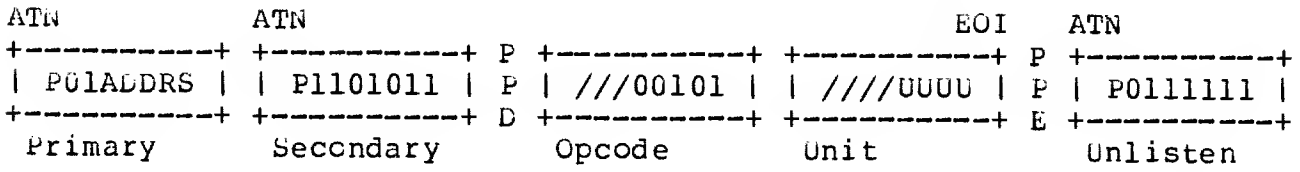
Type: Disc Read

Purpose: The Unbuffered Read Verify is identical to the unbuffered read command except that the margins for good data are reduced. This command gives a high confidence that the data on the disc is correct.

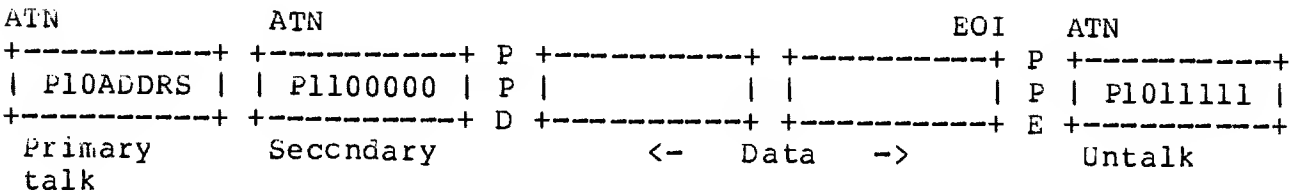
Description: (See Unbuffered Read)

HP-IB Sequence:

REQUEST UNBUFFERED READ VERIFY



SEND DATA



Status: (See Unbuffered Read)

Requirements for Execution: (See Unbuffered Read)

4-50. COLD LOAD READ

Type: Disc Read

Purpose: The Cold Load Read is a command to read from unit 0, cylinder 0 at a specified head and sector address. This command consists of a seek to cylinder 0 followed by a read operation starting at the specified head and sector. Consecutive sectors are read until the Bus Controller stops the read.

Description: Note: The following description of Cold Load Read describes a pseudo unbuffered operation. At the time of the writing of this document a true unbuffered read was being designed. If implemented, refer to future revisions of this document for the correct description.

Following reception of the read command, Parallel Poll is disabled, the DSJ cleared, and the First Status Bit checked. If First Status is set, the format of the diskette is determined and the First Status Bit cleared. If the unit can be accessed the 7902 performs a seek to cylinder 0, reads 1 sector into the internal buffer, then asserts Parallel Poll waiting for the Send Data secondary. After the Send Data secondary is received Parallel Poll is disabled and the buffered sector is sent to the Bus Controller. When the sector has been sent the controller fills the buffer with the next sector from the disc and then sends it to the bus controller. This process is repeated until one of the terminating conditions occur:

a. If the unit becomes unavailable, or a sector cannot be found when the buffer is empty, a byte tagged with EOI is sent.

b. If a CRC error or D Bit is encountered, the sector is sent followed by a byte tagged with an EOI.

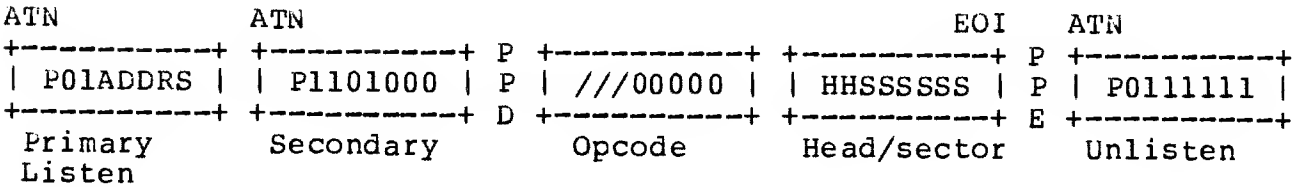
c. If at any time during the operation, the device notices that it has been untalked, or that the Bus Controller has sent a byte, the transfer will be stopped.

Following any of the above terminations, status is updated, and Parallel Poll response is re-enabled. If there was an error in reading data from the disc, the target address is left pointing to the sector in which the error occurred. Otherwise, the target sector points to the sector following the last sector read from the disc.

The Cold Load read uses unbuffered HP-IB protocol, although all sector transfers take place through the buffer. Thus, there is a pause in data flow to the HP-IB each time the buffer is refilled from the disc. This pause occurs at the beginning of the read, and after every sector is transferred. Depending on when the read is started and the staggering of the sectors, see the Format command, this inter sector pause may be up to 160 milliseconds long.

HP-IB Sequence:

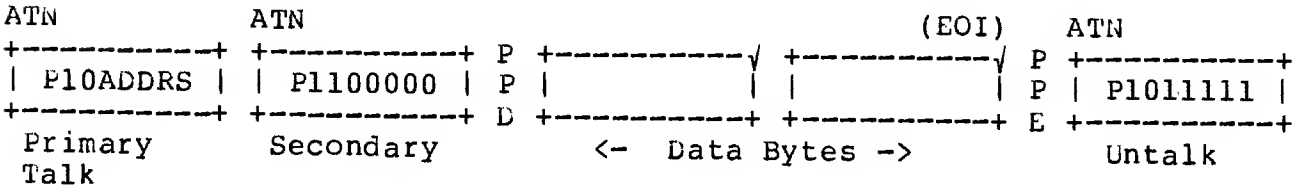
COLD LOAD READ REQUEST



Where: HH - Head Address

SSSSSS - Sector Address

SEND DATA



Status: No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Unsuccessful Read

S1 - Error
S2 - Bits 8, 11 and 13 set if appropriate
DSJ - 1

Requirements for Execution:

a. 2 data bytes in command
b. Unit available

c. Disc ready and present
d. Disc of known format

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB Controller, the Parallel Poll response is assured to be reenabled upon the reception by the device of the Untalk command.

451. ID TRIGGERED READ

Type: Disc Read

Purpose: ID Triggered Read is used to read a sector of which the ID field cannot be found or read correctly. As an example, if the status from a read indicates that the target address sector is not found, the ID Triggered Read would be used to locate and trigger off of the previous sectors ID field to read the target sector. The host processor must be aware of the sector interleaving to request the correct sector to trigger from. (See Format)

Note: ID Triggered Read is only supported for HP format and uses Buffered protocol.

Description:

HP-IB Sequence:

REQUEST ID TRIGGERED READ

ATN	ATN			EOI	ATN
P01ADDRS	P1101011	P	///00110	////UUUU	P0111111
		D			E
Primary listen	Secondary		Opcode	Unit	Unlisten

SEND DATA

ATN	ATN			EOI	ATN
P10ADDR	P1100000	P			P1011111
		D			E
Primary talk	Secondary		<- Up to 1 sector data ->		Untalk

Status: (See Buffered Read)

Requirement for Execution: (See Buffered Read)

4-52. DISC WRITE COMMANDS

4-53. BUFFERED WRITE

Type: Disc Write

Purpose: Data read from the disc is transferred through an internal buffer on the controller before transmitted over the HP-IB to the Bus Controller. This buffering allows the controller to transmit asynchronously from an arbitrarily slow rate to about 110 Kbytes per second. The maximum HP-IB data rate is faster than the data rate from the disc, thus less time is used to transfer 1 sector over the HP-IB then it took to read that sector. During the remaining time the HP-IB is free to be used by other devices on the Bus.

Description: Following reception of the write command, Parallel Poll response is disabled, and status of the specified unit is checked, and the Parallel Poll response is reenabled.

At this time, the Bus Controller should send the Receive Data secondary followed by up to 1 sector of data bytes. After seeing the Receive Data secondary, the 7902 will disable Parallel Poll response, and begin placing data bytes in its buffer. The 7902 will stop accepting bytes after:

a. it receives a byte tagged with an EOI,
b. it has accepted 1 sector.

Note: If less then 1 sector is sent the sector will be filled with data in the buffer from previous operations.

After the buffer has been accepted by the controller the current address is checked with the target address. If they differ, a seek to the target track is performed. This may occur if the actuator has slipped, or if an autoincrement to the next cylinder is required.

If an HP format disc is being used, the 7902 attempts the write the 256 bytes in the buffer to the target sector. If the write completes successfully the target address is incremented by one sector. If the target sector cannot be found, or a D Bit is encountered, the sector is not written and the target track is not incremented.

If an IBM format disc is being used, only 128 bytes from the buffer are written to the disc. If the write completes successfully the target address is incremented by one sector. If the target sector is not found, the sector is not written and the target address not updated.

Note: In IBM format, writing to a sector which has the D Bit on, clears the D Bit.

Parallel Poll is reenabled after the write completes or aborts.

If more than 1 sector is to be written, any number of write commands can be used in succession. The 7902 will update the target address automatically. A write will fail if it follows another write which failed, so there is no chance of an error in the middle of a long transfer going unreported. However, error detection will be quickened if a DSJ is used after each write sequence is completed.

HP-IB Sequence:

BUFFERED WRITE REQUEST

ATN	ATN			EOI	ATN
P01ADDRS	P1101001	P	///01000	////UUUU	P0111111
Primary listen	Secondary	D	Opcode	Unit	E Unlisten

RECEIVE DATA

ATN	ATN			EOI	ATN
P01ADDRS	P1100000	P			P1011111
Primary talk	Secondary	D	<- Data bytes ->		E Unlisten

Status: No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Unsuccessful Write

S1 - Error
S2 - Bits 8, 11 and 13 set if appropriate
DSJ - 1

Requirements for Execution:

a. 2 data bytes in command
b. 0<=UNIT<=3
c. DSJ <> 2
d. Disc present and ready
e. First Status Bit not set
f. Status 1 = Normal completion,
I/O program error, or
illegal opcode error.
g. Disc not write protected

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

4.4. UNBUFFERED WRITE

Type: Disc write

Purpose: The Unbuffered Write allows more than 1 sector to be transferred from the Bus Controller to the disc using a single HP-IB command sequence. Due to the inability to share the HP-IB during the transfer, the Unbuffered Write is not the preferred mode when HP-IB performance is desired.

Description: Note: The following description of Unbuffered Write describes a pseudo unbuffered operation. At the time of the writing of this document a true unbuffered read was being designed. If implemented, refer to future revisions of this document for the correct description.

Following reception of the write command, Parallel Poll response is disabled and status of the specified unit is checked. The 7902 now waits for the Receive Data secondary and then fills its internal buffer with 1 sector from the Bus Controller. When the buffer is full the 7902 searches for the target sector and writes the buffer to it. When the buffer has been emptied, the 7902 accepts another sector from the HP-IB and in turn writes it to the next sector of the disc. This process continues until a byte tagged with an EOI is received, or an error occurs. The buffer containing the byte tagged with the EOI is written to the disc before the write completes.

If an error occurs (i.e., drive goes not ready, a HP format D Bits is encountered, or the sector can't be found, etc.) writing to the disc will stop, but the 7902 will continue accepting bytes until an EOI tagged byte is received.

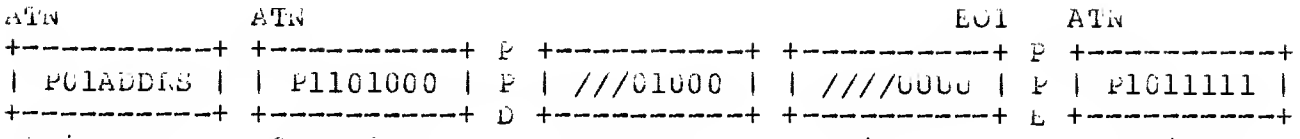
If an error occurs, the target address will point to the sector in which it occurred. Otherwise, the target address will point to the sector following the last sector written. When writing has completed, Parallel Poll response will be reenabled.

As in the Unbuffered Read, Unbuffered Write actually uses the internal buffer on the controller. However, the protocol used is unbuffered in that Parallel Poll is not used to indicate when data may be sent to the 7902. Like unbuffered read, there is a pause in the data flow to the 7902 each time the buffer is written to the disc. The pause occurs after every sector is transferred.

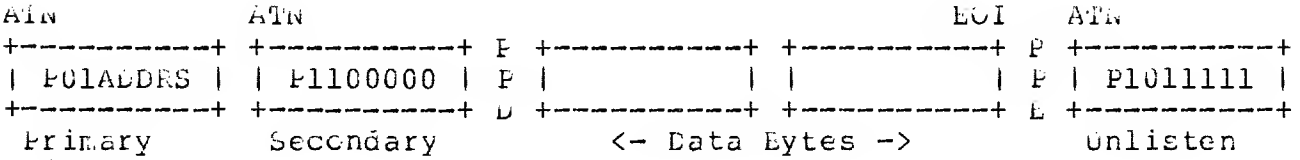
Depending on when the write starts, and the staggering of the sectors (see the Format Commmand), this pause may be up to 160 milliseconds long.

HP-IB Sequence:

UNBUFFERED WRITE REQUEST



RECEIVE DATA



Status: No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Unsuccessful Write

S1 - Error
S2 - Bits 8, 11 and 13 set if appropriate
DSJ - 1

Requirements for Execution: (See Buffered Write command)

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

4-55. INITIALIZE

Type: Disc Write

Purpose: The initialize command is used to set or reset D Bits. It is similar to the buffered write with the following exception:

a. For HP format diskettes, all D Bits on the target track will be set or reset, before the target sector is written.

b. For IBM format diskettes, the D Bits of the target sector is set or reset as the sector is written.

The Initialize command is especially useful wnen used with the Format command to make invisible tracks.

Description: Following reception of the initialize command, Parallel Poll is disabled, and the status of the selected unit is checked.

If an HP format diskette is present, the entire target track is re-formatted, with the D Bit in all sectors set or reset according to the D Bit specified in the opcode byte of the command. This re-formatting has several results:

a. All data on the target track is lost,

b. The sector interleave of the track is changed to type 2 (every other sector),

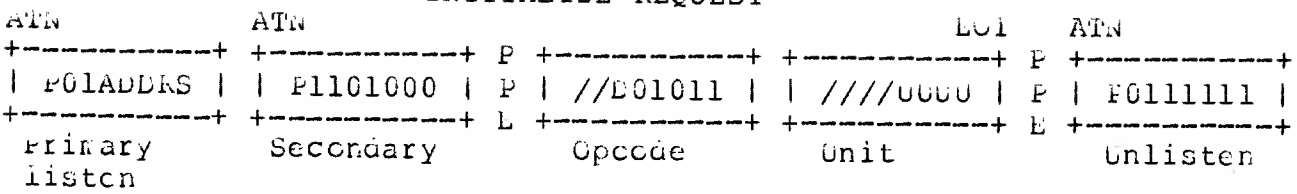
c. The spiral offset of the target track may no longer be optimal.

If an IBM format diskette is present, the D Bit is set or reset according to the D Bit specified in the opcode data byte as each sector is written. The initialization of an IBM sector does not affect the format or data of the remaining sectors of the target track as does an HP format.

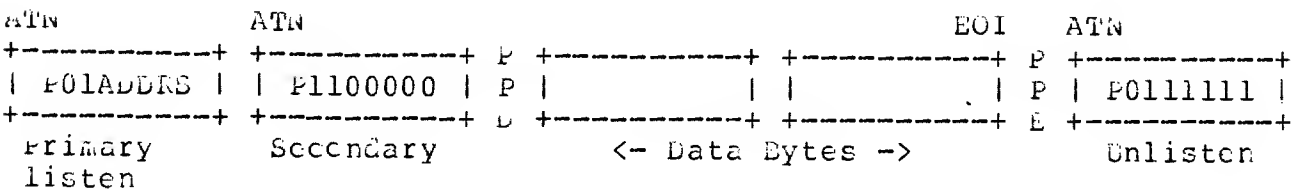
After the Initialize request is sent, the command accepts and writes data in a manner identical to the buffered write command.

HP-IB Sequence:

INITIALIZE REQUEST



RECEIVE DATA



Status: No errors

S1 - 0
S2 - Unchanged
DBJ - 0

Unsuccessful

S1 - Error
S2 - Bits 8, 11 and 13 set is appropriate
DBJ - 1

Requirements for Execution: (See Buffered Write requirement)

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

4-56. FORMAT

Type: Disc Write

Purpose: The Format command is a part of the sequence of commands which takes a diskette which is unformatted or has the wrong format into a disc with a usable format. The 7902 supports three types of formats: HP double density, single or double sided, diskettes, and single sided standard IBM format diskette. The Formatting operation also can make tracks marked with the D Bit into invisible tracks.

The Format sequence was designed to allow the disc controller to do as much of the work of formatting as possible, but still allow the host system to set its own criteria for:

a. Format type,
b. Bad track detection,
c. Sector interleave,
d. Spiral offset,
e. Format data byte.

Description: After receiving the format command, Parallel Poll is disabled, and the status of the specified unit is checked. If the unit can be used, the disc is formatted according to the type, Old Format Override, interleave, and selected data byte.

If the disc is of a different format then the Format command requests, or the Override Old Format Bit is set, the entire diskette will be formatted without invisible tracks.

If the disc is the same type as that requested by the Format command, and the Override Old Format Bit is not set, 7902 will attempt to read from each track before it is formatted and make that track invisible if:

a. the track is already invisible,
b. a sector with a D Bit set if found,
c. the track has no readable sectors.

Note: The 7902 looks at the D Bit of a random sector to decide whether or not to make that track invisible. HP format requires that the D Bit of all the sectors be set, so there is no problem. But, IBM format allows a mixture of set and cleared D Bits on one track. Therefore, before formatting an IBM diskette, all D Bits on a good track should be cleared, and all D Bits on a bad track set.

If the type parameter is set to 2 the diskette will be given HP format. Double sided diskettes will automaticaly be formatted on both sides, and single sided diskette only on head 0. If the type parameter is set to 8 the diskette will be formatted IBM. Double sided diskettes are not supported in IBM format. Single sided diskettes will be formatted on head 0 only (IBM standard). Other values of type will cause a I/O program error.

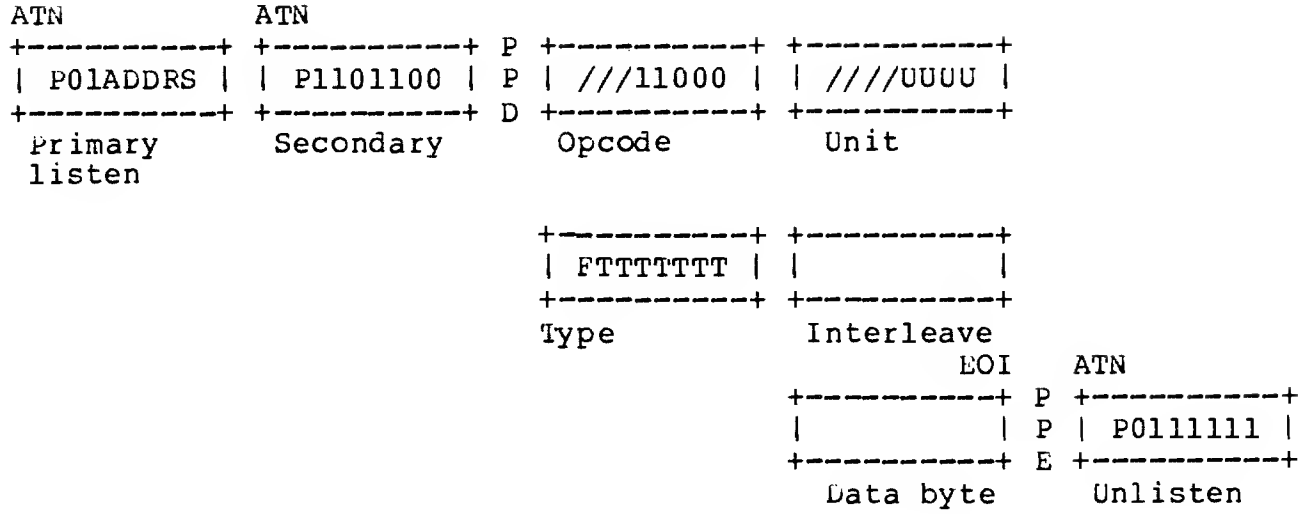
The Interleave parameter determines the order in which the sectors occur on a track. Data transfers which use the internal buffer on the 7902, or host systems that accept data slower than the disc rate, operate more efficiently if the ordering of the sectors is non-sequential. Non-sequential sectors ordering allows for sectors to be arranged on the disc by logical use instead of by physical location.

In general, the Interleave parameter indicates the number of diskette revolutions requiried to send or recieve one tracks worth of data. For example, an interleave value of 5 would indicate that the sectors would be arranged on the diskette in a manner that would require 5 revolutions to read 1 track. Note: At the present time an Interleave parameter value of 2 (2 revolutions per track) generates the sector secquence with the minimum time required to transfer one track.

HP format also uses the Interleave parameter to determine the inter-track spiral offset. This offset minimizes the effect of track to track seeks by physically arranging sector 29 of one track and sector 0 of the next to make the the track seek time approximately the same as the rotational latency.

HP-IB Sequence:

FORMAT REQUEST



Where: ADDRS - 7902 HP-IB address

F - Override Old Format Bit

TTTTTTT - Wanted format type
2 - HP
8 - IBM

Interleave - 1 to 29 for HP
1 to 26 for IBM

Status: No errors

S1 - 0
S2 - Unchanged
DSJ - 0

Unsuccessful

S1 - Error
S2 - Bits 8, 11 and 13 set if appropriate
DSJ - 1

Parallel Poll: The Parallel Poll response is reenabled after the operation is completed, normally or abnormally.

HP Sector Interleave Sequence

A	B	C	Sector Sequence																										
1	6	3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
2	6	3	0	15	1	16	2	17	3	18	4	19	5	20	6	21	7	22	8	23	9	24	10	25	11	26	12	27	13	28	14
3	6	3	0	10	20	1	11	21	2	12	22	3	13	23	4	14	24	5	15	25	6	16	26	7	17	27	8	18	28	9	19
4	6	4	0	15	8	23	1	16	9	24	2	17	10	25	3	18	11	26	4	19	12	27	5	20	13	28	6	21	14	29	7
5	6	5	0	6	12	18	24	1	7	13	19	25	2	8	14	20	26	3	9	15	21	27	4	10	16	22	28	5	11	17	23
6	6	6	0	5	10	15	20	25	1	6	11	16	21	26	2	7	12	17	22	27	3	8	13	18	23	28	4	9	14	19	24
7	7	7	0	13	26	9	22	5	18	1	14	27	10	23	6	19	2	15	28	11	24	7	20	3	16	29	12	25	8	21	4
8	8	8	0	15	4	19	8	23	12	27	1	16	5	20	9	24	13	28	2	17	6	21	10	25	14	29	3	18	7	22	11
9	9	9	0	10	20	7	17	27	4	14	24	1	11	21	8	18	28	5	15	25	2	12	22	9	19	29	6	16	26	3	13
10	10	10	0	3	6	9	12	15	18	21	24	27	1	4	7	10	13	16	19	22	25	28	2	5	8	11	14	17	20	23	26
11	11	11	0	11	22	3	14	25	6	17	28	9	20	1	12	23	4	15	26	7	18	29	10	21	2	13	24	5	16	27	8
12	12	12	0	5	10	15	20	25	3	8	13	18	23	28	1	6	11	16	21	26	4	9	14	19	24	29	2	7	12	17	22
13	13	13	0	7	14	21	28	5	12	19	26	3	10	17	24	1	8	15	22	29	6	13	20	27	4	11	18	25	2	9	16
14	14	14	0	15	13	28	11	26	9	24	7	22	5	20	3	18	1	16	14	29	12	27	10	25	8	23	6	21	4	19	2
15	15	15	0	2	4	6	8	10	12	14	16	18	20	22	24	26	28	1	3	5	7	9	11	13	15	17	19	21	23	25	27
16	16	16	0	15	2	17	4	19	6	21	8	23	10	25	12	27	14	29	1	16	3	18	5	20	7	22	9	24	11	26	13
17	17	17	0	23	16	9	2	25	18	11	4	27	20	13	6	29	22	15	8	1	24	17	10	3	26	19	12	5	28	21	14
18	18	18	0	5	10	15	20	25	2	7	12	17	22	27	4	9	14	19	24	29	1	6	11	16	21	26	3	8	13	18	23
19	19	19	0	19	8	27	16	5	24	13	2	21	10	29	18	7	26	15	4	23	12	1	20	9	28	17	6	25	14	3	22
20	20	20	0	3	6	9	12	15	18	21	24	27	2	5	8	11	14	17	20	23	26	29	1	4	7	10	13	16	19	22	25
21	21	21	0	10	20	3	13	23	6	16	26	9	19	29	2	12	22	5	15	25	8	18	28	1	11	21	4	14	24	7	17
22	22	22	0	15	11	26	7	22	3	18	14	29	10	25	6	21	2	17	13	28	9	24	5	20	1	16	12	27	8	23	4
23	23	23	0	17	4	21	8	25	12	29	16	3	20	7	24	11	28	15	2	19	6	23	10	27	14	1	18	5	22	9	26
24	24	24	0	5	10	15	20	25	4	9	14	19	24	29	3	8	13	18	23	28	2	7	12	17	22	27	1	6	11	16	21
25	25	25	0	6	12	18	24	5	11	17	23	29	4	10	16	22	28	3	9	15	21	27	2	8	14	20	26	1	7	13	19
26	26	26	0	15	7	22	14	29	6	21	13	28	5	20	12	27	4	19	11	26	3	18	10	25	2	17	9	24	1	16	8
27	27	27	0	10	20	9	19	29	8	18	28	7	17	27	6	16	26	5	15	25	4	14	24	3	13	23	2	12	22	1	11
28	28	28	0	15	14	29	13	28	12	27	11	26	10	25	9	24	8	23	7	22	6	21	5	20	4	19	3	18	2	17	1
29	29	29	0	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2

Where:

A - Interleave Value
B - Track to Track offset
C - Head to Head offset

IBM Sector Interleave Sequence

A	Sector Sequence																									
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
2	1	14	2	15	3	16	4	17	5	18	6	19	7	20	8	21	9	22	10	23	11	24	12	25	13	26
3	1	10	19	2	11	20	3	12	21	4	13	22	5	14	23	6	15	24	7	16	25	8	17	26	9	18
4	1	14	8	21	2	15	9	22	3	16	10	23	4	17	11	24	5	18	12	25	6	19	13	26	7	20
5	1	22	17	12	7	2	23	18	13	8	3	24	19	14	9	4	25	20	15	10	5	26	21	16	11	6
6	1	14	10	23	6	19	2	15	11	24	7	20	3	16	12	25	8	21	4	17	13	26	9	22	5	18
7	1	16	5	20	9	24	13	2	17	6	21	10	25	14	3	18	7	22	11	26	15	4	19	8	23	12
8	1	14	11	24	8	21	5	18	2	15	12	25	9	22	6	19	3	16	13	26	10	23	7	20	4	17
9	1	4	7	10	13	16	19	22	25	2	5	8	11	14	17	20	23	26	3	6	9	12	15	18	21	24
10	1	14	9	22	4	17	12	25	7	20	2	15	10	23	5	18	13	26	8	21	3	16	11	24	6	19
11	1	20	13	6	25	18	11	4	23	16	9	2	21	14	7	26	19	12	5	24	17	10	3	22	15	8
12	1	14	12	25	10	23	8	21	6	19	4	17	2	15	13	26	11	24	9	22	7	20	5	18	3	16
13	1	3	5	7	9	11	13	15	17	19	21	23	25	2	4	6	8	10	12	14	16	18	20	22	24	26
14	1	14	3	16	5	18	7	20	9	22	11	24	13	26	2	15	4	17	6	19	8	21	10	23	12	25
15	1	8	15	22	3	10	17	24	5	12	19	26	7	14	21	2	9	16	23	4	11	18	25	6	13	20
16	1	14	6	19	11	24	3	16	8	21	13	26	5	18	10	23	2	15	7	20	12	25	4	17	9	22
17	1	24	21	18	15	12	9	6	3	26	23	20	17	14	11	8	5	2	25	22	19	16	13	10	7	4
18	1	14	4	17	7	20	10	23	13	26	3	16	6	19	9	22	12	25	2	15	5	18	8	21	11	24
19	1	12	23	8	19	4	15	26	11	22	7	18	3	14	25	10	21	6	17	2	13	24	9	20	5	16
20	1	14	5	18	9	22	13	26	4	17	8	21	12	25	3	16	7	20	11	24	2	15	6	19	10	23
21	1	6	11	16	21	26	5	10	15	20	25	4	9	14	19	24	3	8	13	18	23	2	7	12	17	22
22	1	14	7	20	13	26	6	19	12	25	5	18	11	24	4	17	10	23	3	16	9	22	2	15	8	21
23	1	18	9	26	17	8	25	16	7	24	15	6	23	14	5	22	13	4	21	12	3	20	11	2	19	10
24	1	14	13	26	12	25	11	24	10	23	9	22	8	21	7	20	6	19	5	18	4	17	3	16	2	15
25	1	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
26	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26

Where:

A - Interleave Value

SECTION V
CONTROLLER PCA
FUNCTIONAL DESCRIPTION

5-1. INTRODUCTION

This section contains a functional description of controller PCA-A1, part no. 07902-60024. Included are descriptions of each function within the controller, supported by a functional block diagram.

5-2. OVERVIEW OF CONTROLLER PCA-A1

Controller PCA-A1 provides an interface between an Hewlett-Packard Interface Bus (HP-IB) channel and up to four 07902-60025 disc drives. Commands are accepted from the HP-IB channel and interpreted to provide the proper operating sequences for the selected disc drive. This includes providing control and timing signals, sending data to the disc drive, receiving data from the disc drive, and handling all input/output communication with the drive channel. PCA-A1 interprets HP-IB channel commands for seeks, data transfers, and error reporting; provides the control signals to drive PCA-A2; and receives the resulting status information.

If an error occurs, or when a flexible disc is removed or inserted into a disc drive, PCA-A1 requests attention from the HP-IB. PCA-A1 also generates and decodes error detection bits which are recorded with the data. In addition to these normal operations, self-tests are performed on PCA-A1 and any connected disc drives.

Figure 5-1 shows the basic organization of PCA-A1. A processor system occupies the top half of the figure and the bottom half is occupied by a disc drive interface. The processor system includes an HP-IB interface (PHI) chip, a micro-CPU (MC^2) chip, and associated read-only and random-access memories. The disc drive interface circuitry includes a data serializer/ deserializer (SERDES), a cyclic redundancy check (CRC) generator checker, a data decoder, a data encoder, and control and status registers.

5-3. HP-IB INTERFACE

The PHI chip provides a high-speed interface to the HP-IB via PHI/HP-IB converters for the host system and the MC^2. The PHI appears to the MC^2 as a bank of eight addressable registers. All interaction with the HP-IB is performed by reading or writing these registers. In addition, the PHI chip provides buffering for inbound and outbound data through two 8-byte FIFO's which can be accessed by the host processor. The lines provided by the PHI chip for interfacing to the MC^2 include:

- A 10-bit wide data bus.
- Three register select lines for selecting among the eight registers.
- A data direction line for specifying either reading or writing of the selected register.
- Two handshake lines to coordinate data transfer.
- An interrupt line to alert the host processor of selected events.

Four quad instrumentation bus transceivers are used with the PHI chip for interfacing with the HP-IB. Two transceivers are assigned for 8-bit data transfer between the HP-IB and the PHI chip and two are used for HP-IB commands and handshakes.

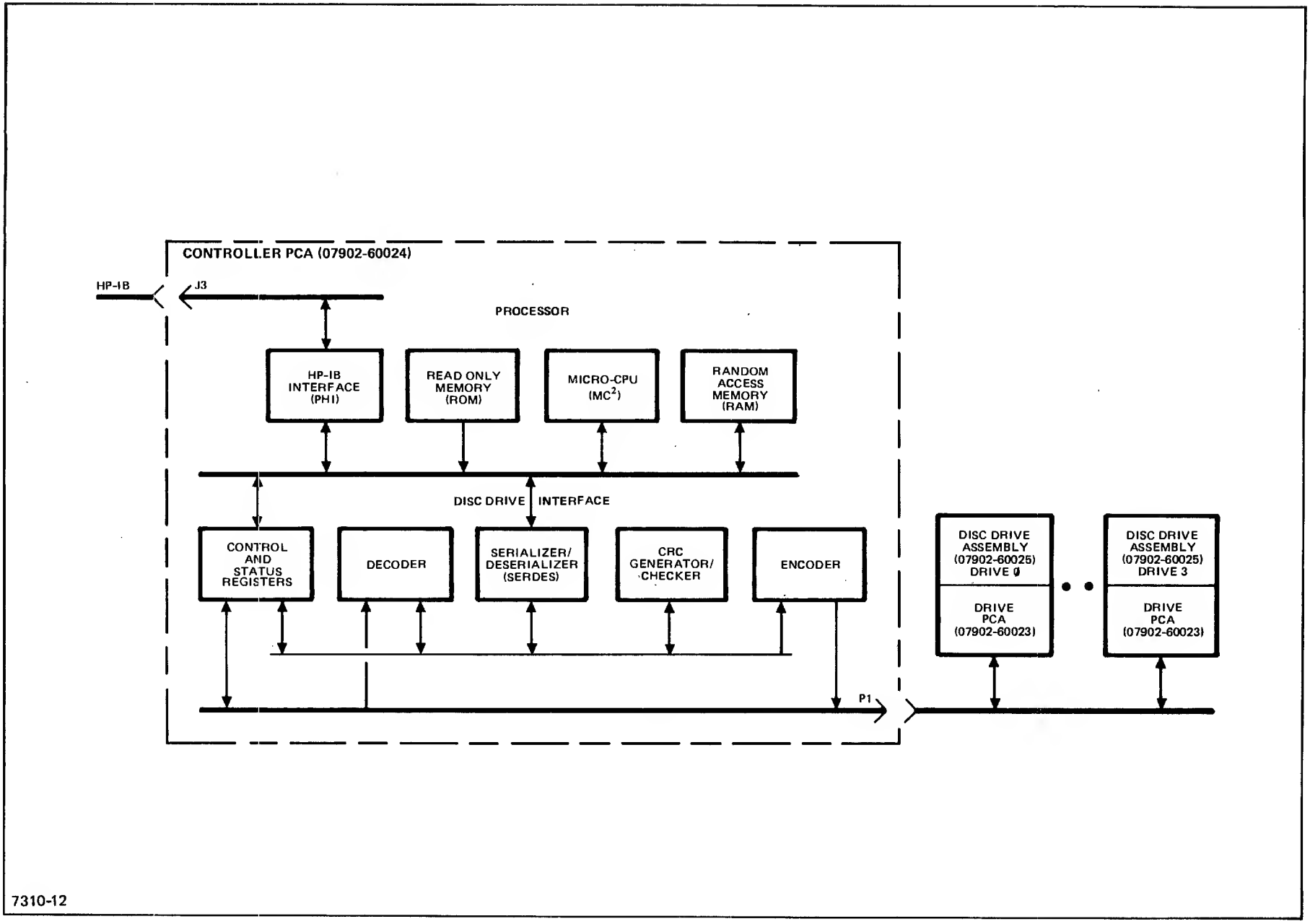


Figure 5-1. Controller PCA-A1 (07902-60024) Block Diagram

5-4. PROCESSOR

The MC^2 chip is a 16-bit parallel, high performance, low power processor that is designed for controller applications. The instruction cycle is typically 0.95 to 2 microseconds to execute any of the fixed width, 16-bit instructions which can process one- four- eight- or 16-bit fields. Operations for logical decision making include direct bit testing of internal and external registers, indexed branches, priority encoder for most significant bit finder, external event synchronization, and a program status register that records salient characteristics of the last produced result.

When the MC^2 has control, data may be moved from the RAM to the HP-IB, from the HP-IB to the RAM, or from the TTL bus to the MC^2. When idle, direct data transfer between the TTL bus and the RAM or the HP-IB is possible. Since the MC^2 contains several internal registers, all other registers on the controller PCA are considered to be external registers. Therefore, when operating on external registers, the program provides appropriate commands to selected registers, using the external control lines.

Two 24-pin 256 × 8 random access memory (RAM) chips are used in PCA-A1. Part of the RAM is called the buffer, part is called the stack, and part is used as a scratch pad. The buffer holds the preamble, data, and postamble either before they are sent to the disc drive or after receiving them from the disc drive. The stack is used when the MC^2 calls up subroutines and the scratch pad is for temporary storage of variables used by the program.

Eight 24-pin, 1024 × 8 read only memory (ROM) chips are used for main program storage, including the self-test program.

5-5. DECODER

When a disc drive is reading from a disc, controller PCA-A1 receives a pulse from every flux transition which is detected on the disc. The decoder synchronizes itself with this pulse train and separates it into clock and data pulses according to the rules of the recording format in use. (Refer to paragraph 4-2 for details of the recording formats.) These pulses are used to generate serial data and serial clock signals which are fed to the SERDES. The decoder consists of a phase-locked loop, a data separator, and some sequencing logic.

5-6. ENCODER

When a write is taking place, the disc drive requires a pulse whenever a transition should be written on the disc. The encoder takes serial data and clock information from the SERDES (or CRC) and converts it to the pulse stream needed by the disc drive. The encoder employs the encoding rules of the format being used. (Refer to paragraph 4-2.) This includes the addition of precompensation when the HP double density format is selected.

For diagnostic purposes, the encoder can be connected directly to the decoder. This allows testing much of the controller hardware without writing on or reading back a flexible disc.

5-7. SERIALIZER/DESERIALIZER

The serializer/deserializer (SERDES) is basically a shift register which converts serial data to parallel data or vice versa. There are two shift registers — one for data and one for clock information. When reading from a disc, serial data and serial clock are shifted into the SERDES. This produces parallel data and parallel clock that the MC^2 can read. When writing to a disc, the MC^2 writes parallel data and clock into the SERDES which then shifts it out to generate serial data and serial clock which are sent to the encoder and CRC circuitry. The SERDES appears to the MC^2 as two registers in the external register bank dedicated to the selected disc drive.

5-8. CRC

In order to allow detection of errors, cyclic redundancy check (CRC) information is recorded along with data on the flexible disc. When writing a field on the disc, the CRC circuitry uses the serial data coming from the SERDES to generate a 16-bit check word. At the end of the field, the check word is sent to the encoder to be written on the disc. When reading from the disc, serial data from the SERDES is fed back into the CRC circuitry. A field of information and its associated check word will leave the CRC circuitry in a known state. Thus, it is possible to determine if an error has occurred by looking at the state of the CRC circuitry after a read has been completed.

5-9. CONTROL AND STATUS REGISTERS

Six registers in the disc external register bank allow the MC^2 to manipulate and test various signals from the controller and the disc drives. This includes MC^2 control of which disc drive is selected, the operation of the head actuator stepping motor, head selection, the self-test LED's, and the operation of the read/write circuitry in the controller. The MC^2 can test the status of the selected drive, the self-test and device address switches, and the status of the read/write circuitry in the controller. In addition to the registers, there is also logic that controls the handshaking with the processor system.

5-10. FIRMWARE

In order to read or write the disc, the MC^2, under firmware control, must sequence the operation of the other parts of the controller. The following sequence is typical of how the data transfers occur.

The firmware constantly monitors the PHI chip, waiting for bytes to arrive from the HP-IB. Incoming bytes are checked to see if they form a command. If a valid read command is received, the data buffer in the RAM is filled with data from the disc. The data is then sent through the PHI chip to the HP-IB. If a write command is received, the buffer is filled with data from the HP-IB. This data is then written to the disc.

In order to transfer data between the data buffer and the disc, the proper sector of the disc must be found. To do this, the read circuitry is enabled to search for the next field on the disc. (Refer to paragraph 4-2 for details of the recording formats.) If a data field is encountered, it is ignored and a new search for the next field is started.

When an ID field is encountered, the track and sector numbers it contains are checked. If the cylinder number is incorrect, the controller attempts to seek to the proper cylinder, and then starts the process again. If the cylinder number is correct, but the sector number is incorrect, the search for the next field is started again. When both the cylinder and sector numbers are correct, the desired sector has been found. Now, if data is to be written on the disc, the entire data field of the sector is rewritten using data from the data buffer.

SECTION VI
DISC DRIVE FUNCTIONAL DESCRIPTION

6-1. INTRODUCTION

This section provides a functional description of disc drive assembly, part no. 07902-60025 and associated drive PCA-A2, part no. 07902-60023. Included are descriptions of the disc drive electromechanical components and the disc drive electronics circuitry.

6-2. GENERAL DESCRIPTION

The disc drive assembly consists of a drive mechanism, read/write heads, a head positioning mechanism, and control interlocks. Drive PCA-A2 includes read and write circuits, control circuits for head positioning and loading, and read, write, and erase enabling.

6-3. DRIVE MECHANISM

The drive mechanism is composed of a drive motor, spindle hub, and drive belt. The drive motor rotates the spindle at 360 rpm through the drive belt. Constant rotational speed is achieved for 60 Hz or 50 Hz primary power by changing the drive motor pulley and belt. A registration hub, centered on the spindle hub, positions the flexible disc. A hub clamp that moves in conjunction with the cartridge guide fixes the flexible disc to the registration hub.

6-4. READ/WRITE HEADS

The read/write heads are single-element ceramic devices with straddle head erase elements to provide erase areas between tracks. The heads, one for each side of the disc, are mounted on a carriage assembly that is positioned by a stepper motor. The flexible disc is inserted through a disc access door on the front of the disc drive and the disc is held in a plane perpendicular to the read/write heads by a plate located on the disc drive frame. During a read/write operation, the heads are in direct contact with the flexible disc.

6-5. HEAD POSITIONING MECHANISM

A mechanism that includes a stepper motor, capstan, and taut metal band positions the read/write carriage assembly on the flexible disc. The stepper motor, driven by signals from drive PCA-A2, rotates in 3.6-degree increments moving the heads one track per increment. The HP-IB channel supplies controller PCA-A1 with head positioning commands which in turn supplies positioning data to PCA-A2.

6-6. DRIVE ELECTRONICS

The drive electronics circuitry is contained on drive PCA-A2 which is attached to the bottom of the disc drive frame. PCA-A2 is connected between controller PCA-A1 and the various electromechanical components of the disc drive thereby providing the necessary interface for disc drive operation. PCA-A2 recognizes when the disc drive is selected and initiates the proper head positioning and loading actions. For write operations, PCA-A2 turns on write and erase current generators and provides the correct write current transitions. During read operations, data obtained from the flexible disc is amplified and conditioned, and sent to controller PCA-A1. PCA-A2 also contains interlock circuits that prevent drive operations when the disc access door is not closed and latched, the heads are not loaded, or the flexible disc is write protected. In addition, PCA-A2 makes available status information.

6-7. FUNCTIONAL DESCRIPTION

The following paragraphs provide a functional description of the circuits on drive PCA-A2 and the operation of the associated disc drive electromechanical components. Refer to figure 6-2 for a detailed functional block diagram of PCA-A2.

The circuits on PCA-A2 are divided into four principle systems: a control system, a head positioning system, a read/write system, and a power supply filtering system. The control system provides the interface between controller PCA-A1 and the disc drive, the head actuating system moves and loads the read/write heads in response to signals from PCA-A1, the read/write system reads information from or writes information onto the surface of the flexible disc, and the power supply filtering system filters and distributes the dc voltages from the host system.

6-8. INPUT/OUTPUT SIGNALS

There are 14 signals input to drive PCA-A2 from controller PCA-A1, five signals output from PCA-A2 to PCA-A1, and two input/output (bidirectional) signals between PCA-A2 and PCA-A1. These signals, together with identifying mnemonics, are described in table 6-1.

6-9. LOGIC SIGNAL NOTATION

In the disc drive logic circuits, a signal is applied to its destination at all times in one of two states: active or inactive. A signal is active when the voltage level (high or low) is such as to make the action occur for which the signal was intended. This action is usually identified by the signal mnemonic. To indicate the active voltage level of the signals, the mnemonics for all active high signals have an "H" suffix and the mnemonics for all active low signals have an "L" suffix. Table 6-2 uses an active high signal (REDYH) and an active low signal (TRKOL) to summarize the details of the signal notation system.

Table 6-1. Drive PCA-A2 Input/Ouput Signals

MNEMONIC	SIGNAL	FUNCTION
OUTPUT TO CONTROLLER PCA		
INDXL	Index	Active when index hole in flexible disc passes index photodetector. Signal is active once per revolution of disc (6 times/second).
REDYH	Ready	Active when disc drive is in a ready state, i.e., a disc is in drive and spinning, drive is selected, heads are loaded, and head 1 is not selected with a single-sided disc.
SPINL	Spinning	Becomes active after a Reset Spinning (RSPNH) if the disc drive is nominally up to speed. Also alerts controller PCA to removal and insertion of a new flexible disc.
TRK0L	Track Zero	Active when read/write heads are positioned at track zero (outermost track used on disc).
WPRTL	Write Protect	Active when flexible disc in disc drive is write protected (allows reading only).
INPUT FROM CONTROLLER PCA		
DLCKL	Door Lock	When active and held by control latch, locks disc access door (without regard to heads being loaded).
DSLVL	Drive Select Valid	When active, validates Drive Select signals DSL0H, DSL1H, and DSL2H.
DSL0H, DSL1H, DSL2H	Drive Select	Binary-coded decimal signals used to identify disc drive with which controller desires to communicate.
HDACTL	Head Load	When active and held by the control latch, signal enables stepper, loads heads, and locks door.
HED1H	Head One	When active and held by the control latch, it selects head 1. When inactive, head 0 is selected.
LDCTL	Load Control	When active, with drive selected and not in a write mode, clocks the control latch which latches input signals HDACTL, PHIBH, PHIAH, DLCKL, and HED1H on the drive PCA.
PHIBH PHIAH	Phase B Phase A	When held by control latch, generates signals which drive stepper motor in head actuator assembly.
PONH	Power On	When active, enables the control gates that activate the write circuits. Write is allowed if drive is selected and ready, write mode is selected, and disc drive does not contain a write-protected flexible disc.
PORH	Power On Reset	When active, resets control latch index counter and spinning flip-flop. This reset action disables stepper, unloads heads, unlocks door, selects head 0, and makes SPINL inactive.

Table 6-1. Drive PCA-A2 Input/Output Signals (Continued)

MNEMONIC	SIGNAL	FUNCTION
INPUT FROM CONTROLLER PCA (Continued)		
RSPNH	Reset Spinning	When active, clocks output of the Index Counter into the spinning (SPINH) flip-flop.
WRITL	Write	When active, places disc drive in write mode.
OUTPUT TO/INPUT FROM CONTROLLER PCA		
DATAH DATAL	Data	Bidirectional differential lines carrying read and write information to and from the controller PCA.

Table 6-2. Logic Signal Notation

SIGNAL MNEMONIC	VOLTAGE LEVEL	STATE	MESSAGE TRANSMITTED
REDYH	high	active	Drive ready
REDYH	low	inactive	Drive not ready
TRKOL	low	active	Read/write heads at track 0
TRKOL	high	inactive	Read/write heads not at track 0

6-10. CONTROL SYSTEM

The control system responds to inputs from controller PCA-A1 and places the disc drive in a write mode or a read mode. In addition, the system provides PCA-A1 with drive status information. To ensure that the drive mechanism is in the correct condition for reading and writing, the control system also monitors the state of four photodetector sensors and a door-closed switch in the drive mechanism. The actions of the various circuits comprising the control system are discussed in the following paragraphs.

6-11. DRIVE SELECT. To permit controller PCA-A1 to communicate with one disc drive at a time, each disc drive is assigned an identity number between 0 and 7. PCA-A1 uses this number to select the disc drive with which it desires to communicate. Drive PCA-A2 employs a comparator to decode the identity number. The comparator compares the state of binary-coded decimal Drive Select inputs DSL0H, DSL1H, and DSL2H from PCA-A1 with BCD inputs from the front panel Drive Select switch. If the coding of the two sets of inputs coincide, and Drive Select Valid signal DSLVL is active, the drive select circuit outputs Drive Select signal DSLH. If a Drive Select switch is not connected to PCA-A2, the circuit defaults to 0.

6-12. DOOR CLOSED DETECTOR. The disc drive assembly contains a door-closed switch which is activated by the disc guide assembly. The switch has two output lines: Door Open and Door Closed, both of which are active low. The Door Closed line is active when the disc access door on the front of the disc drive is closed and latched. The active Door Closed signal causes the door closed detector on drive PCA-A2 to output an active high Door Closed signal. When the disc access door is open, the active Door Open signal resets the detector, causing the output to become inactive.

6-13. WRITE PROTECT DETECTOR. The write protect detector is a phototransistor assembly mounted on the disc guide assembly. The purpose of the detector is to sense if the write protect slot in the cover of a flexible disc inserted into the drive is open or covered by a tab. (Write protect is enabled when the slot is open — refer to paragraph 3-4 for details.) The output of the photodetector is coupled to an interface circuit on drive PCA-A2. The output of the interface is active when the write protect slot is open. The output signal from the interface inhibits the write operation by gating off the write interlock which in turn prevents operation of the write current and erase current sources. The output of the write protect photodetector can be observed at a test point labeled WPRTH.

6-14. TRACK ZERO DETECTOR. The track zero detector is a phototransistor assembly mounted on the main casting of the disc drive. The purpose of the detector is to sense when the read/write carriage assembly reaches track 00. The phototransistor output is active for tracks −01, 00, and 01, and inactive for tracks 02 and above. The phototransistor output is connected to an interface circuit on drive PCA-A2. The interface output is AND'ed with the head actuator stepper motor phase $\overline{A}$ and $\overline{B}$ drive lines to develop a unique track 0 signal. The signal, identified as TRK0L, is coupled via a line driver to controller PCA-A1. The output of the interface circuit, before it is AND'ed with phases $\overline{A}$ and $\overline{B}$, can be observed at a test point labeled TK0H.

6-15. SINGLE-/DOUBLE-SIDED DISC INDEX DETECTOR. The index detector assembly consists of two phototransistors mounted on the disc guide assembly. The purpose of the index detector is to sense the presence of the index hole in the flexible disc. One phototransistor senses the index hole of a single-sided disc and the other phototransistor senses the index hole of a double-sided disc. The two outputs from the phototransistors are coupled to an interface circuit on drive PCA-A2. The two interface outputs are OR'ed together to give one output which can be observed at a test point labeled INDEXH. When either a single-sided or double-sided disc is rotating in the disc drive, signal INDEXH is a pulse which occurs once per revolution of the disc. Signal INDEXH is a) connected to an index counter, and b) coupled via an inverting line driver to controller PCA-A1 as signal INDXL. The separate outputs from the interface, before they are OR'ed, can be observed at test points labeled INDEX0L (one-sided disc index pulse) and INDEX1L (double-sided disc index pulse).

6-16. SINGLE-SIDED DISC DETECTOR. The purpose of the single-sided disc detector is to inform controller PCA-A1 when a single-sided disc is inserted into the disc drive. The detector monitors the state of single-sided disc index signal INDEX0L from the index detector. When INDEX0L is active, the single-sided disc detector output SSDH is active. The detector is reset at power-on and when the disc access door is opened.

6-17. INDEX COUNTER. The index counter provides Disc Spinning signal SPINH which is active when certain disc drive operating conditions are valid. These conditions are: disc loaded, disc access door closed and latched, and the occurrence of two successive index pulses (an indication that the disc is rotating). The index counter also returns disc drive status information to controller PCA-A1.

The index counter consists of three D-type flip-flops connected in cascade. The clear input to all three flip-flops is derived from the output of the door closed detector and an inverted Power On Reset (PORH) input. As long as the disc access door is open, the clear line is held low and no circuit action can occur. The Q output of the third flip-flop, connected via an inverting line driver to PCA-A1, is status signal SPINL. Signal SPINL is inactive at this time since the clear input to the flip-flop holds its Q output low.

As soon as a disc is loaded into the disc drive and the disc access door is closed and latched, the clear line goes high and allows the first two flip-flops to start counting. When a second index pulse occurs, the second flip-flop a) lights an LED labeled B (disc ready) on drive PCA-A2 and the DISC READY LED on the optional front panel indicator display, and b) pulls the D-input of the third flip-flop high. When PCA-A1 checks the status of the disc drive, it pulses the Reset Spinning (RSPNH) line. This action clocks the third flip-flop, causing its Q output to go high. Status signal SPINH is now active. Signal SPINH is also used internally in the PCA-A2 circuitry that determines if the disc drive is ready.

6-18. **DRIVE READY.** Several signals in the drive PCA-A2 circuitry are gated together to produce status signal Drive Ready (REDYH). The following conditions must be true for REDYH to become active:

- SPINH active, i.e., a flexible disc has been inserted into the disc drive, the disc access door is closed and latched, and the disc is spinning.
- Drive selected with signal DSLH active.
- Heads loaded.
- Head 1 not selected if a single-sided flexible disc is in the disc drive.

Drive Ready (REDYH) is coupled via a line driver to controller PCA-A1.

6-19. **READ ENABLE.** The read mode of operation is enabled when Drive Ready signal REDYH is active and the Write (WRITL) input is inactive. These conditions enable a) the output of the read circuit, and b) the driver section of the data transceiver.

6-20. **WRITE ENABLE.** The write mode of operation is enabled when Drive Ready signal REDYH is active, the Write (WRITL) input is active, and the Write Protect (WPRTH) line is inactive. These conditions enable the write interlock circuit.

6-21. WRITE INTERLOCK. The write interlock supplies drive to the current switches in the write current and erase current sources when the write enable signal is active. However, operation of the write interlock is inhibited if the Power On (PONH) line is inactive. Both PONH and write enable must be active in order to enable the write interlock. Signal PONH, generated in the host system power supply, is inactive when the ac line voltage input to the supply falls below its low limit specification.

6-22. FRONT PANEL DISPLAY DRIVERS. The front panel display drivers provide drive for three LED's on an optional front panel indicator display that can be connected to PCA-A2 via connector A2J6. (Refer to paragraph 2-8 for details of this display.) The LED's are labeled DRIVE SELECTED, DISC READY, and WRITE PROTECTED. The DRIVE SELECTED LED is driven by signal HDACTH from the control latch; the DISC READY LED is driven by the Q output of the second flip-flop in the index counter; and the WRITE PROTECTED LED is driven by a signal from the write protect interface. Two LED's on PCA-A2 are also activated by the front panel display drivers. These LED's are labeled A (drive selected) and B (disc ready).

6-23. HEAD ACTUATING SYSTEM

The function of the head actuating system is to load the read/write heads on any one of the 77 tracks on the flexible disc, select either of the two read/write heads for a read/write operation, and lock the disc access door to prevent removal of the flexible disc while the heads are loaded. The system circuits on drive PCA-A2 include a control latch, a head unload delay circuit, a head load driver, a stepper driver, and a door lock driver. Associated electromechanical components on the disc drive assembly include a head load solenoid, a head actuator assembly with stepper motor, and a door lock solenoid.

6-24. CONTROL LATCH. The control latch retains inverted Head Actuate (HDACTL), Stepper Phase (PHIAH, PHIBH), Door Lock (DLCKL) and Head Select (HED1H) information received from controller PCA-A1. The latch is clocked by the Load Control (LDCTL) signal from PCA-A1, AND'ed with Drive Select (DSLH) and an inverted Write (WRITL). These signals prevent a) the latch from clocking in new information when the drive is not selected or if it is in a write mode, and b) accidental stepping to other tracks when the disc drive is writing on a particular track.

The control latch is reset by the Power On Reset (PORH) input from PCA-A1. When reset, the latch is in a state whereby the heads are unloaded, the stepper motor is disabled, the disc access door is unlocked, and head 0 is selected.

6-25. HEAD UNLOAD DELAY. The head unload delay circuit delays unloading of the heads for approximately 1.5 seconds after the Head Actuator (HDACTL) signal becomes inactive. This allows the disc drive to respond without any settling delay to another head load command occurring less than 1.5 seconds after the previous one ended. The HDACTL signal from the control latch is input to a 1.5-second delay circuit, the output of which is OR'ed with HDACTL. When HDACTL is active, it loads the heads via the OR gate output. When HDACTL becomes inactive, the output of the delay circuit remains active for a further 1.5 seconds, continuing to load the heads for this period. The output of the OR gate also enables the stepper motor driver circuit.

6-26. HEAD LOAD DRIVER. The head load driver provides drive to the head load solenoid which, when activated, allows the heads to contact the surface of the flexible disc. The head load driver is energized when the HDACTH signal from the head load delay circuit is active *and* the output of the second flip-flop in the index counter is active. This gating ensures that the heads cannot be loaded without having a flexible disc in the disc drive. The input to the head load driver can be monitored at a test point labeled HDLDL.

6-27. STEPPER DRIVER. The stepper driver provides drive for the 4-phase 3.6-degree per step permanent magnet stepper motor driving the head actuator assembly. The rotary motion of the stepper motor is transformed into linear motion by an actuator mechanism that employs a capstan and taut metal band. Each 3.6-degree step of the motor increments the head position one track.

The 4-phase coils of the stepper motor are connected to form two pairs of 2-phase coils in parallel. Current is driven into the pairs in either direction according to the stepping sequence desired. To switch the direction of current through the coils, the stepper drivers must be able to source current or sink current. Each driver pair is enabled such that one is the inverse of the other. Controller PCA-A1 supplies two phase inputs to drive PCA-A2. These are labeled Phase A (PHIAH) and Phase B (PHIBH). The control latch outputs non-inverted and inverted phase signals QA, $\overline{QA}$, QB, and $\overline{QB}$ to the stepper driver. The stepping sequence for the actuator stepper motor is shown in figure 6-1. The stepper motor driver is enabled by the output of the head unload delay circuit described in paragraph 6-25.

6-28. DOOR LOCK DRIVER. The door lock driver, when energized, energizes a door lock solenoid that holds the disc access door locked by disengaging the latch of the door opening button. The solenoid is energized by either a Door Lock (DLCKL) signal or a Head Load (HDLDL) signal. An LED on PCA-A2 labeled D (door lock) monitors the input signal to the door lock driver.

6-29. HEAD SWITCH. The head switch circuit selects read/write head 0 or head 1 by grounding the center tap of the selected head. This grounding action forward biases diodes in the input circuit of the read preamplifier allowing it to pick up the output of the selected head. When in the write mode the grounding forward biases diodes in the write current source and the erase current source, allowing the sources to supply current to the selected head. The two outputs from the head switch circuit can be monitored at test points H0CTL (head 0) and H1CTL (head 1).

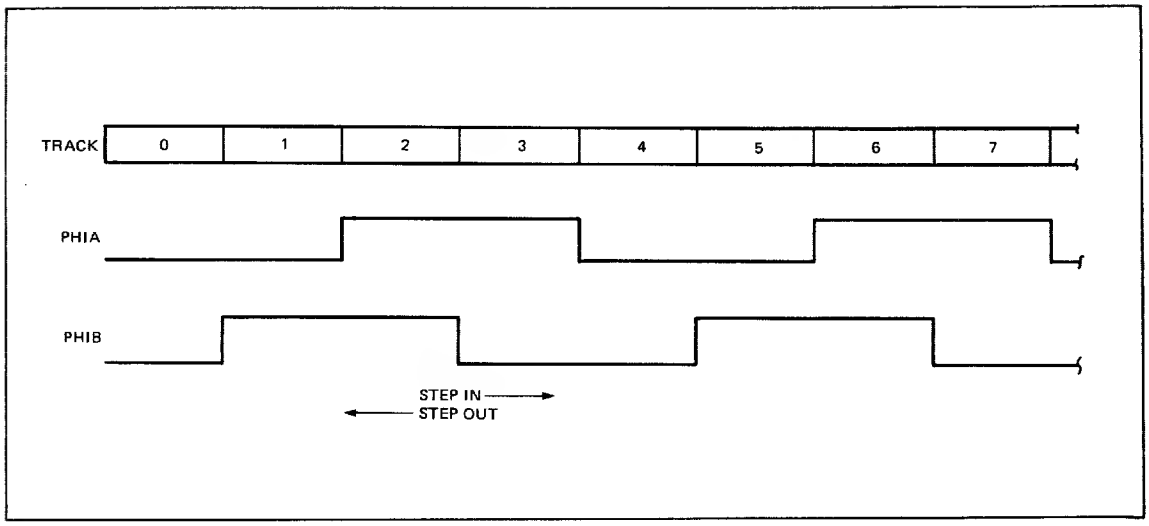


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Figure 6-1. Stepper Motor Switching Sequence

6-30. READ/WRITE SYSTEM

The function of the read/write system is to provide the means to read information from or write information onto the surface of the flexible disc. Included in the following paragraphs are functional descriptions of the read/write heads, the read mode of operation, and the write mode of operation.

6-31. READ/WRITE HEADS. Each read/write head is a gapped ferrite core housed in a ceramic shoe (or slider). The head rides in direct contact with the surface of the disc. Two read/write windings are wound around the core. The windings are connected to a common point and phased such that the common point acts as a center tap. The windings are used for both reading and writing by detecting or providing a magnetic flux change at the gap in the ferrite core. An erase coil, wound on a yoke spanning the track being written by the read/write head, provides a constant magnetic field perpendicular to the read/write head. The erase coil is energized during the write operation and results in the outer edges of the track being trim erased. The erase head ensures that the track being recorded does not exceed the 0.012-inch track width. It also allows for minor deviations in read/write head current so that as one track is recorded it will not "splash over" to adjacent tracks.

Each data bit/clock pulse written is directed to alternate read/write coils, thus causing a change in the direction of current flow through the read/write head. The alternate switching will cause a change in the flux field of the core for each bit. The current through either of the read/write coils will cause the previously recorded information on the disc to be erased as new information is recorded.

On a read operation, as the flux field direction changes on the disc surface as it passes under the core gap, current will be induced into the windings of the read/write head. This current will result in voltage output pulses of differing polarity. When the next bit passes under the gap, another flux reversal in the recording surface takes place. This flux change reverses the induced head current, causing a polarity reversal of the voltage output pulses.

6-32. READ MODE OPERATION. As the surface of the flexible disc moves under the data head, the magnetically stored flux fields intersect the gap in the ferrite core of the head. The motion of the flux reversals passing the head gap causes a current to be induced into the read/write windings wound around the core. The resulting voltages are converted to pulses and coupled to controller PCA-A1 where they are analyzed to define the data recorded on the surface of the disc. Each flux field reversal, caused by a write current polarity change, generates a readback voltage pulse.

6-33. READ CIRCUIT. The read circuitry on drive PCA-A2 is enabled in the read mode. A differential signal from the selected read/write head is coupled via a cable to the input of a read preamplifier stage. The input of the read circuit is isolated from the write current source by isolating diodes. The output of the preamplifier is coupled through a balanced lowpass filter to a differentiator stage. The preamplifier signals at the output of the filter can be observed at test points labeled PREAMP + and PREAMP −. The differentiator stage transforms the read waveforms such that the data points are represented by zero crossings rather than the peaks produced at the data head. The output of the differentiator can be viewed at test points labeled DIFF + and DIFF −.

The output of the differentiator stage is connected to the input of a zero-crossing detector. The detector is a TTL bipolar one shot that produces pulses for positive- or negative-going zero crossings. The output of the zero-crossing detector is connected to a droop detector. This circuit detects false zero crossings caused by droop in the differential output. The droop detector allows only valid output pulses from the zero crossing one-shot to pass through. The output of the detector can be viewed at a test point labeled READ DATA. An LED labeled C (read), also connected to the output of the droop detector, is dimly lit when the disc drive is in the read mode and there is data on the flexible disc.

The output of the droop detector is connected to the driver section of a data transceiver for transmission via differential lines to controller PCA-A1.

6-34. WRITE MODE OPERATION. Information is written on the disc by passing a current through the windings of the read/write head. The current generates a flux field across the gap in the ferrite core, causing the iron oxide particles coated on the recording surface of the disc to be magnetized. The writing process orients the poles of each magnetized particle to permanently store the direction of the flux field as the oxide passes under the head. The direction of the flux field is a function of the polarity of the write current. A data bit/clock pulse is written by reversing the write current through the head windings. This change in write current polarity switches the direction of the flux field across the gap. Erasing old data is accomplished by writing over any data which may have been previously written on the disc.

6-35. WRITE CURRENT. The write circuit consists of a complementary write current source and an erase current source, both of which are enabled when the write mode is selected.

Data bits/clock pulses are input to drive PCA-A2 from controller PCA-A1. (Encoding is performed by circuits on PCA-A1.) The information is applied via the receiver section of the data transceiver to the clock input of a toggle flip-flop in the write current source. The flip-flop produces two complementary signals (Q and $\overline{Q}$) that activate the write current source. The source consists of two transistor current amplifiers, one for each winding on the selected read/write head. The complementary outputs of the flip-flop alternately turn on each source. The switching action selects the head winding through which current will pass. A transistor switch in the write current source, controlled by the write interlock, supplies +12 Vdc to the source when conditions for the write mode of operation are valid.

A light-emitting diode labeled E (write), connected to the Q output of the toggle flip-flop, is dimly illuminated when the write mode is selected and the flip-flop is being toggled by signals from the receiver section of the data transceiver.

The erase current source consists of a single transistor that supplies dc current to the erase winding on the selected read/write head. Operation of the erase current source is controlled by the write interlock.

6-36. POWER SUPPLY FILTERING

Drive PCA-A2 is powered by dc voltages supplied by the host system via connector A2J5. The input voltages are +12 Vdc, +5 Vdc, and −12 Vdc. A −5 Vdc three-terminal negative regulator located on drive PCA-A2 and powered by the −12 Vdc input supplies a −5 Vdc regulated potential. The four voltages are filtered and then distributed throughout drive PCA-A2. The disc drive spindle motor is powered by ac voltage obtained by cable directly from the host system.

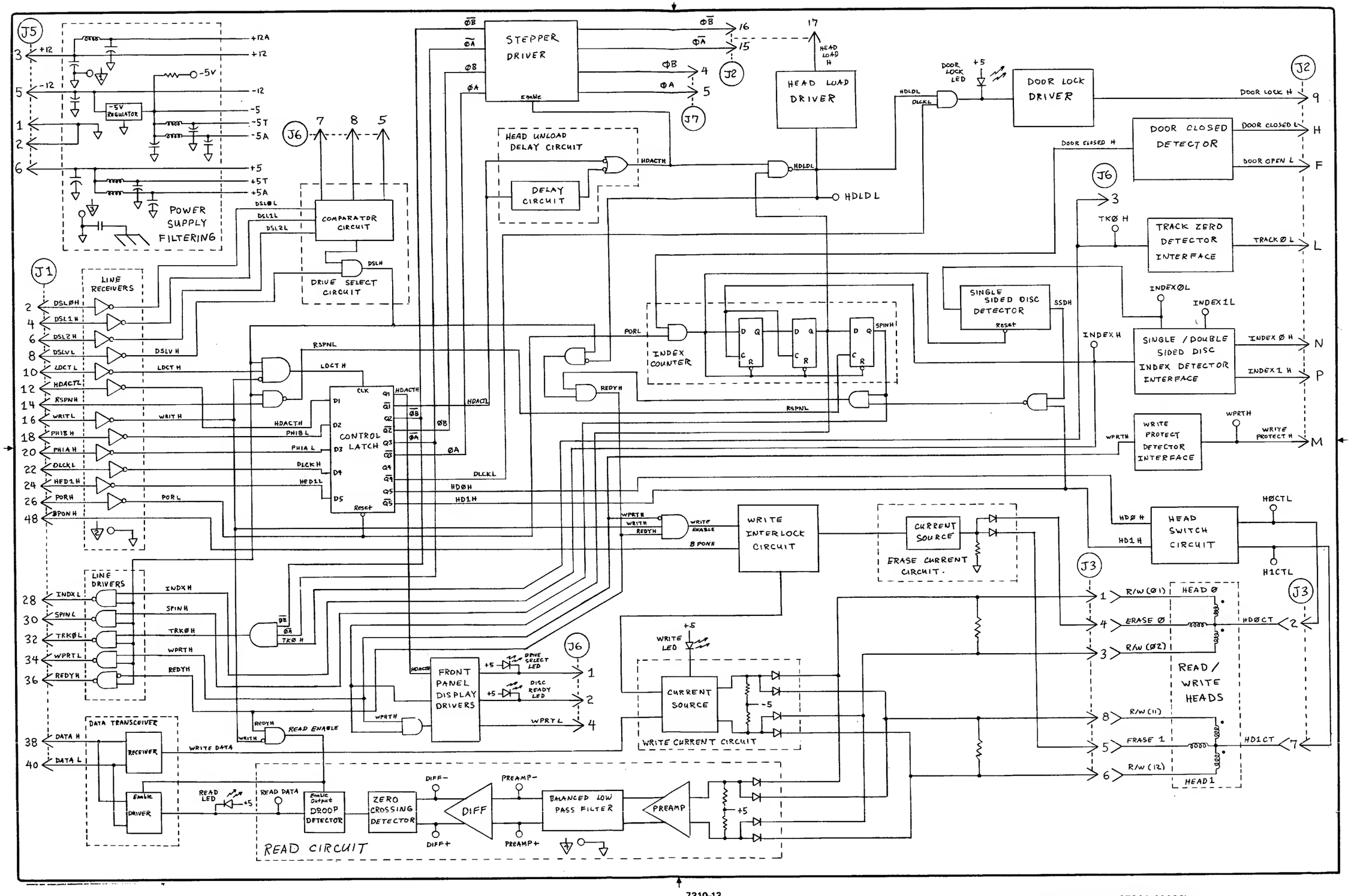

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Figure 6-2. Drive PCA-A2 (07902-60023) Detailed Functional Block Diagram

SECTION VII
MAINTENANCE

7-1. INTRODUCTION

This section contains a listing of the standard and special tools and test equipment required to service the 07902-60025 disc drive, the preventive maintenance schedule, and all required preventive maintenance inspection and cleaning procedures.

WARNING

- **To avoid personnel injury and/or damage to equipment, observe all warnings and cautions stated in this publication and as detailed below.**

- **Use extreme caution when working on the disc drive with power applied. Hazardous voltages are present inside the disc drive whenever it is connected to an active ac power source.**

- **Do not attempt to remove or change printed circuit assemblies (PCA's) or interconnecting cables without first removing power from the disc drive.**

CAUTION

- Never attempt to swing open the cartridge guide assembly without first unloading the heads from the head load bail. Refer to paragraph 9-8 for instructions.

- Never allow the heads to touch each other. Whenever the heads are unloaded from the head load bail, place a piece of clean lens tissue between the heads to prevent them from touching.

- Ensure that the head load actuator up stop adjustment is properly set. This ensures that the flexible disc will clear the heads when it is loaded into the disc drive. Refer to paragraph 9-15 for adjustment instructions.

- Ensure that the door lock assembly is functioning properly. This ensures that the flexible disc cannot be removed from the disc drive while the heads are loaded.

- The read/write heads are factory aligned with a four-track offset between the heads. Loosening the head-mounting screw will destroy this offset and necessitate the return of the disc drive for realignment.

- Do not lubricate the disc drive — oil will cause dust and dirt to accumulate.

- Do not touch the heads or attempt to clean them.

7-2. SERVICE TOOLS AND TEST EQUIPMENT

The following paragraphs list those standard and special tools and test equipment required to service the disc drive.

7-3. STANDARD TOOLS

Table 7-1 lists the standard tools required to service the disc drive. Equivalent tools may be used, when necessary.

Table 7-1. List of Standard Service Tools

TOOL	HP PART NO.
Extractor, Pin (or paper clip)	—
Nutdriver, 1/4-inch socket	8720-0002
Nutdriver, 11/32-inch socket	8720-0004
Pliers, Diagonal Cutting	8710-0006
Pliers, Long Nose	8710-0016
Screwdriver, slot drive, 4 x 1/4-inch	8720-0001
Screwdriver, slot drive, 3 x 3/16-inch	8730-0019
Screwdriver, Pozidriv, 4-inch	8710-0900
Screwdriver, Pozidriv, 3-inch	8710-0899
Soldering Iron	8690-0011
Soldering Iron Tip	8690-0021
Wrench Set, Hex Key	8720-0019

7-4. STANDARD TEST EQUIPMENT

An oscilloscope (HP 1707B Oscilloscope or equivalent) is the only piece of standard test equipment required to service the disc drive. The oscilloscope is used primarily to check the alignment of various components in the disc drive and for troubleshooting.

Note: All oscilloscope sensitivity settings specified in the procedures given in this section and in section IX assume the use of 10:1 oscilloscope probes. If 1:1 probes are used, the sensitivity settings should be scaled accordingly.

7-5. SPECIAL TOOLS

Table 7-2 lists the special tools required to service the disc drive. Substitutions must not be made.

Table 7-2. List of Special Service Tools

TOOL	HP PART NO.
Alignment Flexible Disc	9164-0111
Cartridge Guide Adjustment Tool	1150-1310
Bail Adjustment Tool	1535-3875
Disc Service Unit	12748-60008

7-6. SPECIAL TEST EQUIPMENT

7-7. DISC SERVICE UNIT. The Disc Service Unit (DSU), part no. 12748-60008 is the only item of special test equipment required to service the disc drive. It is used for on-site preventive maintenance, alignment, adjustment, and troubleshooting of the disc drive.

The DSU provides the means to simulate controller PCA-A1 signals to the disc drive and process disc drive responses. Simulated signals are produced either manually or automatically to operate the disc drive. Modes of operation include seek to track, alternate seek, single step, and writes. A numerical keypad and 3-digit numerical display permits selection of test parameters including drive number, alternate seek minimum and maximum track addresses, seek to track address, and track-to-track seek time. Self-test circuitry contained in the DSU is activated at power turn-on and provides a visual indication of the DSU serviceability.

7-8. DSU INSTALLATION. To install the DSU, proceed as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Disconnect the cable from connector J1 (2, figure 10-1) on drive PCA-A2.

c. Connect the ribbon cable connector on the DSU cable to J1 on drive PCA-A2.

d. Connect the 3-pin connector on the DSU cable to J8 (16, figure 10-1) on drive PCA-A2. Ensure that the connector is correctly oriented. The slots in the connector should be facing upward, away from the component side of PCA-A2.

CAUTION

Ensure that the disc drive does not contain a flexible disc at power turn-on. Failure to observe this precaution may result in accidental erasure of data from a nonwrite-protected disc.

e. Restore power to the disc drive as described in paragraph 9-2.

7-9. DSU OPERATING INSTRUCTIONS

Figure 7-1 identifies the DSU front panel controls and indicators and table 7-3 defines the functions of these components. An abbreviated instruction set for the DSU is given in table 7-4 and additional operating instructions are provided in the following paragraphs.

7-10. POWER TURN-ON. At DSU power turn-on, the DSU performs a self-test. If the self-test fails, the 3-digit readout on the DSU displays "bAd" and the keypad is disabled. If self-test passes, all DSU LED's, with the exception of those controlled by the disc drive (INDEX, RD/WR DATA, DRIVE READY, TRACK 0, and WRITE PROTECTED), are lit for 5

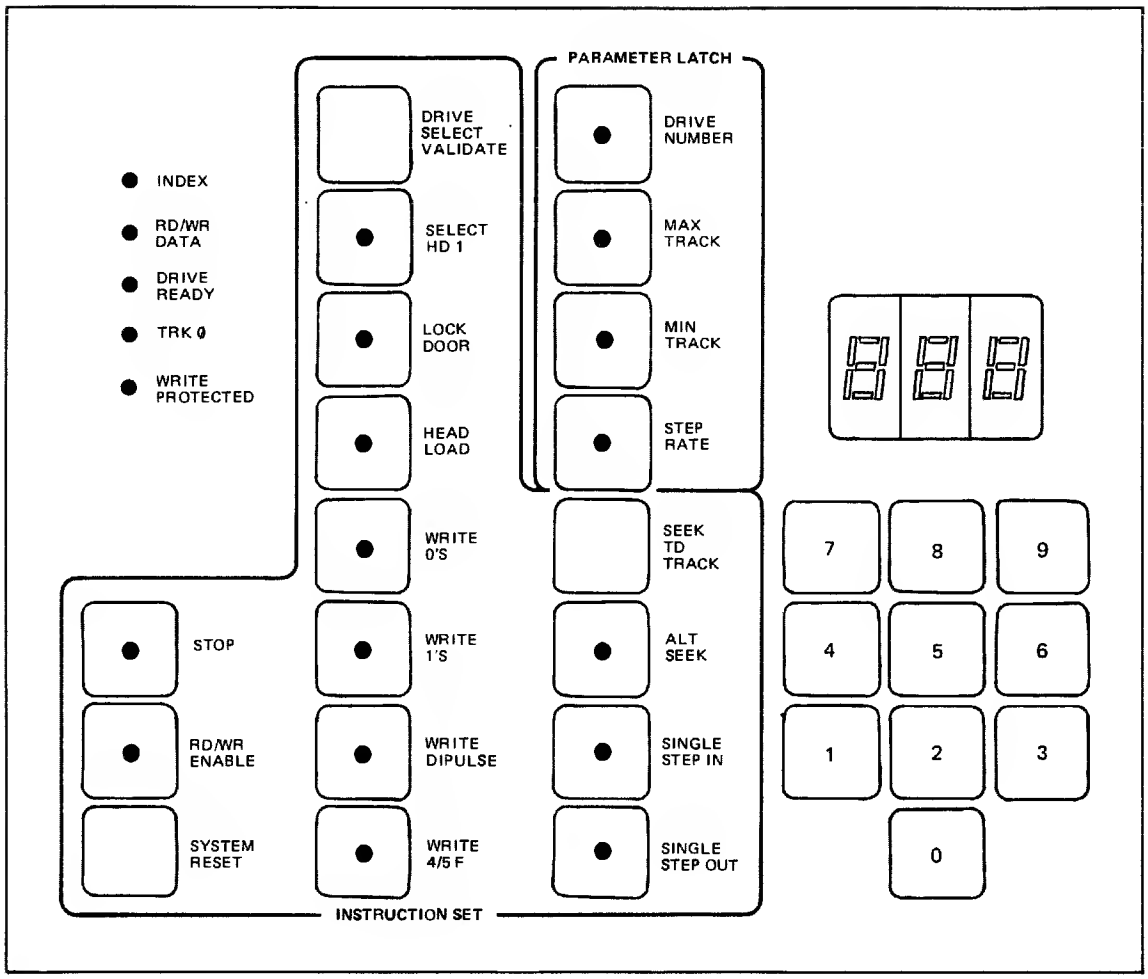

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Figure 7-1. Disc Service Unit Front Panel Controls and Indicators

Table 7-3. Disc Service Unit Controls and Indicators

Decimal Keypad	—	Programs value for drive number, maximum and minimum tracks (alternate seek), step rate, and seek to track parameters. Each time a key is pressed, that number is entered into least significant digit of 3-digit decimal display and other numbers shift up. The programmed number is entered when appropriate parameter pushbutton is pressed. At power turn-on and reset, 3-digit readout is reset to 0.
PARAMETER LATCH pushbuttons		
DRIVE NUMBER	—	Enters keypad number selected for drive number. Pushbutton indicator flashes if number is greater than 7. Selection of a new number automatically recalibrates drive.

Table 7-3. Disc Service Unit Controls and Indicators (Continued)

MAX TRACK	—	Enters keyboard number selected for alternate seek maximum track number. Pushbutton indicator flashes if number is less than current alternate seek minimum track number. At power turn-on and reset, number is automatically set to 76.
MIN TRACK	—	Enters keypad number selected for alternate seek minimum track number. Pushbutton indicator flashes if number is more than current alternate seek maximum track number. At power turn-on and reset, number is automatically set to 0.
STEP RATE	—	Enters keypad number in milliseconds selected for track-to-track seek time. Pushbutton indicator flashes if number is less than 3. At power turn-on and at reset, number is automatically set to 3.
	INSTRUCTION SET pushbuttons	
SEEK TO TRACK	—	Disc drive seeks to track number selected by keypad. If number selected is greater than 76, disc drive seeks to track 76. At power turn-on and reset, track 0 is automatically selected. (Keypad is reset to 0.)
ALT SEEK	—	Disc drive seeks between keypad selected minimum and maximum track numbers. Pushbutton indicator is lit during seek operation. At power turn-on and reset, altemate seek is automatically set to occur between tracks 0 and 76.
SINGLE STEP IN	—	Head assembly steps inward one track. Pushbutton indicator lights if heads are at innermost track (76).
SINGLE STEP OUT	—	Head assembly steps outward one track. Pushbutton indicator flashes if heads are at outermost track (0).
STOP	—	Stops DSU continuous operations (alternate seek, continuous write) and error signals. Pushbutton indicator lights when DSU is waiting for a command.
RD/WR ENABLE	—	Resets disc drive status signal (Spinning). Pushbutton must be pressed at power turn-on or when a disc is removed during a test before DSU operation can continue. Pushbutton indicator in switch lights when Spinning signal is in asserted state.
SYSTEM RESET	—	Resets entire system and disc drive. DSU self-test is initiated and disc drive is recalibrated and initialized.
WRITE 0'S	—	Writes 0's (250 kHz) on disc. Pushbutton indicator lights when write 0's is selected.

Table 7-3. Disc Service Unit Controls and Indicators (Continued)

WRITE 1'S	—	Writes 1's (500 kHz) on disc. DSU pushbutton indicator lights when Write 1's is selected.
WRITE DIPULSE	—	Writes dipulses on disc. Pushbutton indicator lights when write dipulses is selected.
WRITE 4/5 F	—	Writes at 200 kHz on disc. Pushbutton indicator lights when write 4/5 F is selected. Note: If a WRITE pushbutton is pressed and released in less than 1.5 seconds, write lasts for one revolution of the disc; longer than 1.5 seconds produces a continuous write.
DRIVE SELECT VALIDATE	—	Validates drive number. Pushbutton indicator is lit when drive number is validated.
SELECT HD 1	—	Selects head. When pushbutton indicator is lit, head 1 is selected; when indicator is off, head 0 is selected. At DSU power turn-on and reset, head 0 is selected.
LOCK DOOR	—	Locks the front door. When pushbutton indicator is lit, door is locked. At DSU power turn-on and reset, door is unlocked.
HEAD LOAD	—	Loads the heads. Heads are loaded when pushbutton indicator is lit. At DSU power turn-on and reset, heads are unloaded. Pushbutton must be pressed before a seek to track, alternate seek, or single step in/out operation can be initiated, assuming drive is selected.
		LED'S
INDEX	—	Lights each time index hole in disc passes disc drive index sensor. LED operation is gated by disc drive selected (SELECT DRIVE number entered and DRIVE SELECT VALIDATE pressed).
RD/WR DATA	—	Lights when DSU is writing on or reading from a disc.
DRIVE READY	—	Lights when disc drive is ready to be exercised. It also lights when disc drive is not selected.
TRK 0	—	Lights when heads are at outermost track. LED operation is gated by disc drive selected.
WRITE PROTECTED	—	Lights when a write protected disc is in disc drive. Write operations are inhibited. LED operation is gated by disc drive selected.

Table 7-3. Disc Service Unit Controls and Indicators (Continued)

Test Points		
INDEX	—	Output of disc drive index sensor. Signal is active high.
RD/WR DATA	—	Disc drive data signal.
HEAD LOAD	—	Disc drive head load signal. Signal is low when heads are loaded.
+5V	—	+5 Vdc supplied to DSU.
GND	—	+5 Vdc ground.

seconds. The disc drive is now recalibrated and initialized and the DSU is reset. Reset conditions for the DSU include SELECT HD 1, LOCK DOOR, and HEAD LOAD pushbuttons in a non-asserting state; no WRITE condition selected,STOP LED lit; DRIVE NUMBER = 7; MAX TRACK = 76; MIN TRACK = 0; STEP RATE = 3; and keypad display = 0.

Note: Self-test may not occur at power turn-on if application of dc voltage is slow. In this event press the SYSTEM RESET pushbutton to initiate self-test.

7-11. DRIVE SELECT. To select a drive, enter the desired drive number on the keypad display and then press the following pushbuttons: DRIVE NUMBER, DRIVE SELECT VALIDATE, RD/WR ENABLE, and HEAD LOAD.

7-12. EXERCISING DRIVE. The heads must be loaded before a seek to track, alternate seek, single step in/out, or write operation can be performed. The heads are loaded when the HEAD LOAD pushbutton indicator is lit.

7-13. ALTERNATE SEEK. AT DSU power turn-on, the DSU is automatically set to perform alternate seeks between tracks 0 and 76 when the ALT SEEK pushbutton is pressed. To change the track limits requires the use of the MAX TRACK and MIN TRACK pushbuttons as described in table 7-3. Alternate seek is halted with the STOP pushbutton.

Table 7-4. Disc Service Unit Instruction Set

DSU INSTRUCTION SET

Connect DSU to disc drive and apply power. Insert flexible disc, close door, select drive number, press DRIVE NUMBER, DRIVE SELECT VALIDATE, RD/WR ENABLE, and HEAD LOAD.

I. OPERATING MDDES

MDDE	DESCRIPTION	PRDCEDURE
System Reset	First a DSU self-test is performed. If self-test passes, DSU is reset and disc drive is recalibrated and initialized. DSU reset includes HEAD LOAD, LOCK DOOR and SELECT HD 1 inactive; MIN TRACK = 0; MAX TRACK = 76; STEP RATE = 3; DRIVE NUMBER = 7; and Keypad = 0. If self-test fails, 3-digit readout indicates "Bad", and Keypad is disabled.	a. Press SYSTEM RESET. Note: System reset also occurs at DSU power-on.
Seek to Track	Carriage steps to selected track address and stops.	a. Select desired track-to-track step rate on Keypad and press STEP RATE. b. Select desired track number on Keypad. c. Press SEEK TO TRACK.
Single Step In/Out	Operator may single step carriage inward one track or outward one track.	a. Press SINGLE STEP OUT or SINGLE STEP IN, as desired.
Alternate Seek	Carriage steps from one selected extreme track address to other selected extreme track address.	a. Select desired minimum track number on Keypad and press MIN TRACK. b. Select desired maximum track number on Keypad and press MAX TRACK. c. Select desired track-to-track step rate on Keypad and press STEP RATE. d. Press ALT SEEK. e. Press STOP to stop alternate seek.
Write	0's or 1's (250 kHz or 500 kHz) can be written on a scratch flexible disc to check write circuits. Dipulse and 4/5F (200 kHz) writing is also possible.	a. Seek to desired track. b. Select desired head with SELECT HD 1 pushbutton. c. Press desired WRITE pushbutton. Note: If a WRITE pushbutton is pressed and released in less than 1.5 seconds, write lasts for one revolution of disc; longer than 1.5 seconds produces a continuous write. d Press STOP to stop continuous write.

II. DPERATING FEATURES

FEATURES	DESCRIPTIDN	PROCEDURE
Decimal Keypad	Programs values for drive number, seek to track, min. and max. tracks (alternate seek) and step rate parameters. At DSU power turn-on and system reset, readout is reset to 0.	a. Set desired number on 3-digit display. b. Press appropriate PARAMETER pushbutton to enter number into DSU.
Drive Select	Selects drive number (0 - 7).	a. Select desired drive number on Keypad. b. Press DRIVE NUMBER c. Press DRIVE SELECT VALIDATE.
INDEX LED	Lights each time index hole in disc passes disc drive index sensor.	None
INDEX TP	Monitors output of disc drive index sensor. Signal is active high.	None
RD/WR DATA LED	Lights when DSU is writing on or reading from a disc.	None
RD/WR DATA TP	Monitors disc drive read/write signal.	None
TRK Ø LED	Lights when heads are at outermost track.	None
WRITE PROTECTED LED	Lights when a write protected disc is in disc drive.	None
DRIVE READY LED	Lights when disc drive is ready to be exercised.	None
HEAD LOAD TP	Active low when heads are loaded.	None

7-14. PREVENTIVE MAINTENANCE SCHEDULE

The disc drive is designed for a minimum of preventive maintenance. A schedule for periodic inspection of the disc drive is provided in table 7-5. It is recommended that the procedures listed in the schedule be performed at 12-month intervals. Also, the head radial alignment check (paragraph 7-17) must be performed when the disc drive is integrated into the host system and at installation of the host system. The general operation of the disc drive should be verified before regular scheduled maintenance is performed and again after it has been completed. Run the appropriate diagnostic tests in accordance with the instructions provided in the host system diagnostic manual.

Table 7-5. Preventive Maintenance Schedule

ITEM	ROUTINE
Actuator Assembly	Remove all oil, dust, and dirt. Do not clean unless absolutely necessary.
Belt	Check for frayed or weakened areas. Replace if necessary.
Base	Remove all dust and dirt. Check for loose screws, connectors, and switches.
Read/Write Heads	Check for proper azimuth and radial alignment. Refer to paragraphs 7-15 through 7-17. **CAUTION** Do not touch or attempt to clean the heads.

7-15. HEAD AZIMUTH AND ALIGNMENT CHECKS

The following paragraphs contain instructions for testing head azimuth and radial alignment. Since the heads are not field replaceable, failure to meet any one or more of the specifications listed for these tests will necessitate replacement of the disc drive assembly.

7-16. HEAD AZIMUTH TEST

An aximuth test on the heads of the 7902A is now available with the use of the new alignment disc, 9164-0111. This test checks the offset of each head from the perpendicular to the tangent of the track. It should be performed any time read errors occur or when there is incompatibility between discs and drives.

To perform this test requires version No. 360/2A (9164-0111) of the alignment disc. There is a unique pattern on track 76 to measure the amount of angular offset of the head gap to the track. An offset deviation of + or − 18 minutes is the maximum allowable. The following procedures check that the drive is within these limits.

a. Set the oscilloscope controls as follows:

   Sweep: .5 msec/div

   Sensitivity: .1 volts/div

   Input: DC

   Display: A + B, B inverted

   Trigger: Normal, external, +

b. Connect the A-channel probe to TP Diff+ B-channel probe to TP Diff− and the EXT TRIG probe to TP INDEX.

c. Insert the Alignment Disc into the drive to be aligned, and close the drive door.

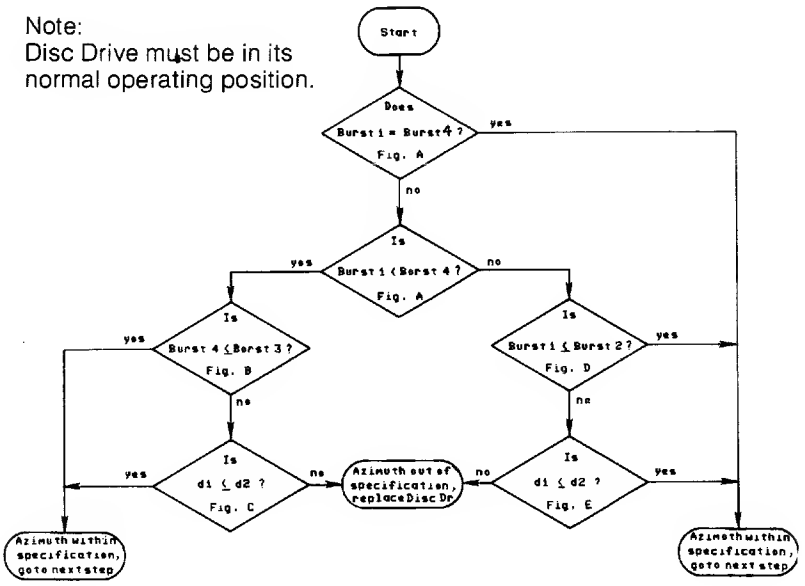
d. With the DSU, select the drive to be aligned, seek to track 76, and select head 0 and do a continuous read.

NOTE

The disc drive unit under test must be in its normal operating position, i.e., horizontal or vertical. Failure to properly position the drive will result in errors in the azimuth measurement.

---

e. Follow the flowchart below. Reject the disc drive or continue to step f as directed by the flowchart.



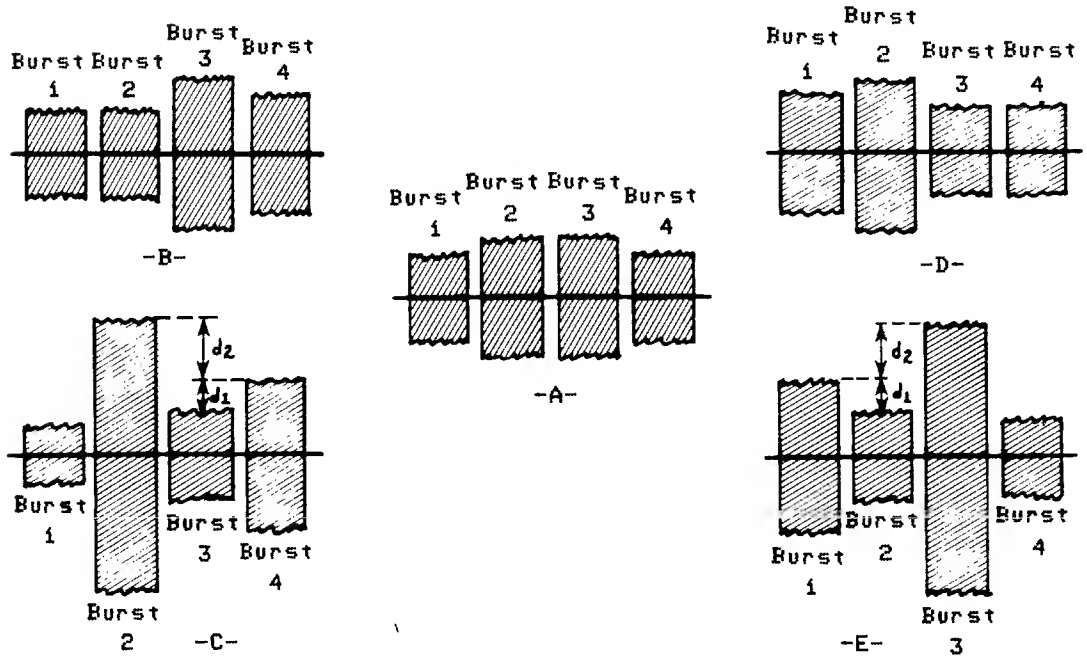


Figure 7-3. Azimuth Test Waveforms

f. Repeat steps d and e for HEAD 1.

7-17. HEAD RADIAL ALIGNMENT CHECK

The head radial alignment is factory set and adjustment is not normally required. To check head radial alignment, proceed as follows:

NOTE

Due to variations in disc size with temperature and humidity, approximately 20 minutes should be allowed for the Alignment Disc to stabilize at the ambient room conditions. For best results, the disc should be removed from the PSP and taken out of its protective jacket as soon as you arrive at the test site. This lets the disc acclimate as fast as possible. The longer you can wait, the more accurate the test results.

---

a. Insert alignment disc, part no. 9164-0111 into the disc drive.

b. Step to track 38, select head 0 and do a continuous read.

c. Using 10:1 probes, connect an oscilloscope to the following test points on drive PCA-A2:

Channel A — PREAMP +
Channel B — PREAMP −

Use drive PCA-A2 INDEX H test point for oscilloscope sync and GND 3 test point for signal ground.

d. Set the oscilloscope controls as follows:

Sweep — 20 msec/div
Sensitivity — 0.01 volt/div
Input — DC
Trigger — EXT, DC, +, NORM
Display — A + B, INV B

e. Make an estimate of the relative humidity in the room where the drive is operating, i.e. is it low (8% to 39%), medium (40% to 59%), or high (60% to 80%).

f. Compare the waveform with that shown in Figure 7-2: Head Radial Alignment Waveforms. Use the following limits when checking the waveforms.

LOW HUMIDITY (8% to 39%): The left lobe amplitude must be between 65% and 105% of the right lobe amplitude.

MEDIUM HUMIDITY (40% to 59%): The smaller lobe amplitude, either left or right, must be at least 80% of the larger lobe amplitude.

HIGH HUMIDITY (60% to 80%): The right lobe amplitude must be between 65% and 105% of the left lobe amplitude.

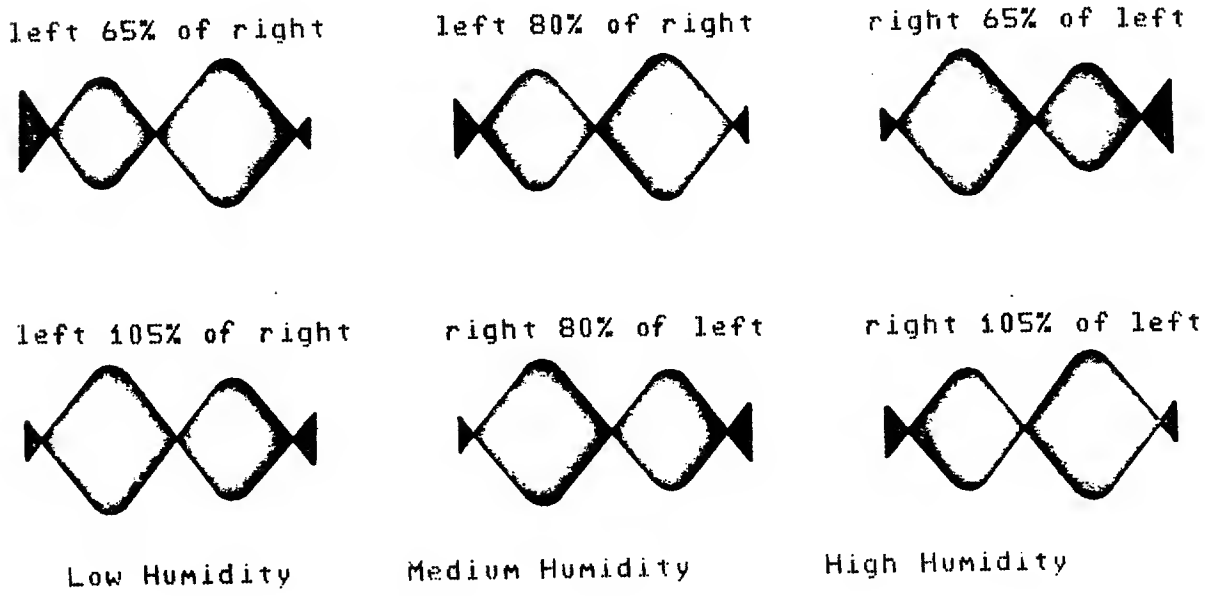


Figure 7-2: Head Radial Alignment Waveforms

g. Loosen the two mounting screws (15, figure 10-3) securing the motor plate to the support bracket.

h. Move the plate by rotating the eccentric adjustment nut (16).

i. When the lobes are within specification, tighten the motor mounting screws.

j. Check the adjustment by stepping off track 38 and returning to it. Check in both directions.

k. Select head 1 and check that the amplitude of the two lobes is within specs. If the lobes are out of specification, repeat steps g through j. It will now be necessary to select head 0 and recheck the lobes. Continue the adjustment until the lobe amplitudes for both head 0 and head 1 are within specification.

l. If the specified waveforms cannot be obtained, replace the disc drive.

m. Following satisfactory adjustment of the head radial alignment, perform the track 0 detector adjustment procedure described in paragraph 9-23.

SECTION VIII
TROUBLESHOOTING

8-1. INTRODUCTION

This section contains troubleshooting information, including a description of self-tests and a summary of the LED readout patterns that indicate particular self-test failures.

WARNING

The HP 7902A Disc Drive does not contain operator-serviceable parts. To prevent electrical shock, refer all troubleshooting activities to service-trained personnel.

8-2. SELF-TEST OVERVIEW

Self-test is a firmware procedure implemented in controller PCA-A1 to check its functional operation. The self-tests can be executed in the following three ways:

- Power-On Sequence. At power-on, controller PCA-A1 executes a power-on sequence that includes self-test.

- Remote, Programmatically. The HP-IB channel can execute the INITIATE SELF-TEST command. Once initiated, the self-test will proceed until either a hard error is detected, or a soft error is detected, or the test completes correctly.

  Note: A hard error will prevent the controller from going on line; a soft error will allow the controller to go on line at the end of self-test.

- Local, Manually. The user may execute self-test by operating the Self-Test switch located on the front of controller PCA-A1. See figure 8-1 for the location of the Self-Test switch and associated self-test controls and indicators.

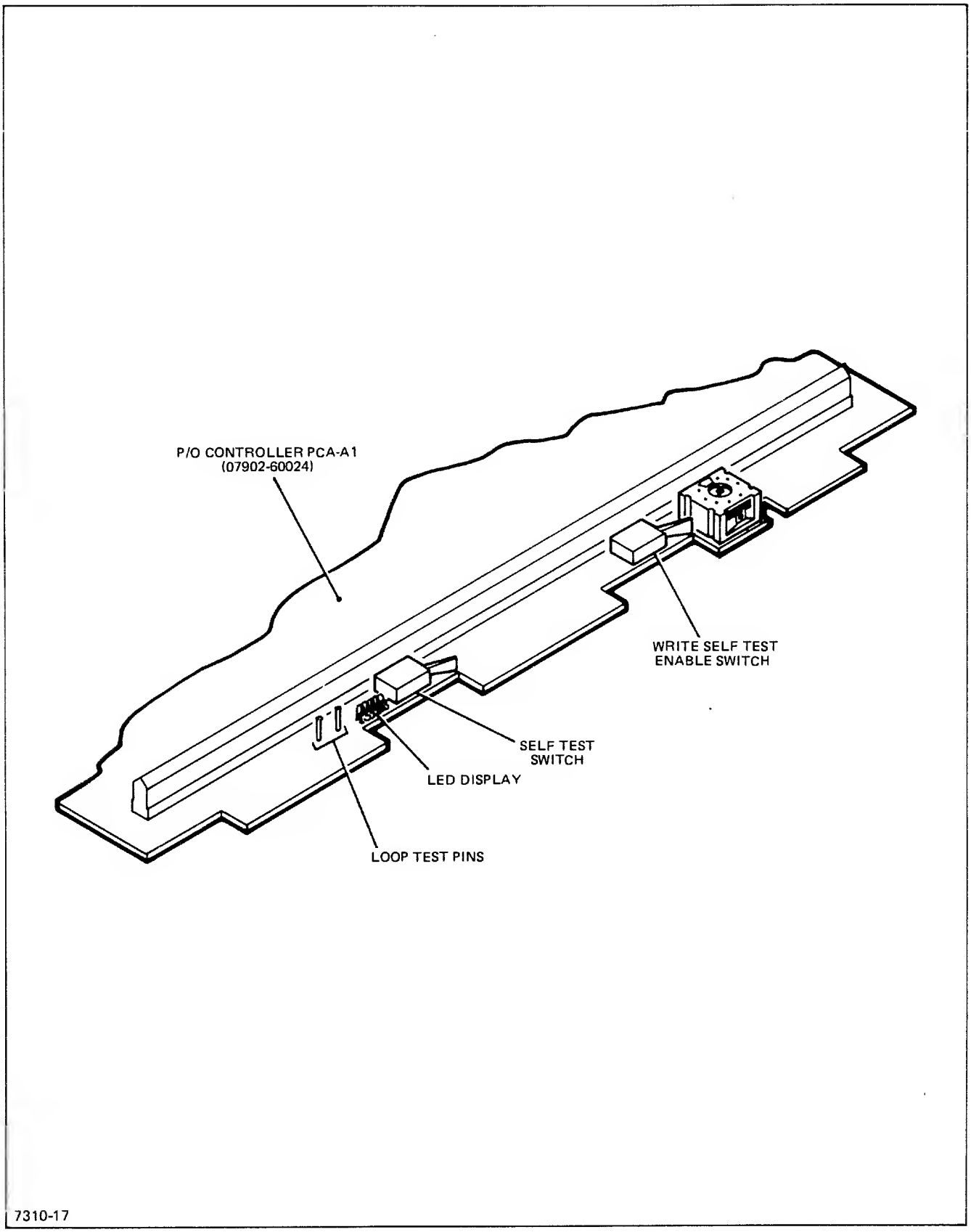


Figure 8-1. Controller PCA-A1 (07902-60024) Self-Test Controls and Indicators

8-3. MANUAL INITIATION OF SELF TEST

After power has been applied to the controller the self test procedure can be initiated and controlled through self test switch, loop pin, and write test switch.

The self test switch is mounted on the left or top side of the controller board next to the LED pack. It is used to initiate self test. To do this, depress the switch; this should cause the LED pattern test to start, the signal that self test has begun. After self test is initiated, the self test switch fuction changes. The new function is dependent upon the state of the loop pin and write test switch.

The loop pin is the set of two test pins mounted to the immediate left of the LED pack. It is used to control the execution cf self test to loop on the failing test or on the entire test if there is no failure. Its function is dependent on the state of the self test switch. The loop pins are termed 'on' when the two pins are connected together.

The write test switch is mounted on the controller board next to the HP-IB device address thumbwheel switch. It is used to command self test to append the write and read tests after the normal self test. Caution: All data on the test cylinder will be lost. To initiate self test with the appended write and read tests the write test switch must be held in while the self test switch is depressed. Once self test has started the state of the write test switch has no meaning and may be released.

8-4. TEST SELECTION

There are three tests selectable in the manually invoked self test, they are:

a. Default self test,
b. Self test with write/read test appended,
c. Self test with read only test appended.

DEFAULT SELF TEST

The default self test is selected by momentarily depressing the self test switch. Once self test has started the self test switch must be released. At this point one pass of the self test procedure is executed then the controller will go online. If an error is found self test will pause for 20 seconds and display the number of the failing test in the LED's, then go online. If no error is found self test will pause for 10 seconds displaying the end-of-self-test number (00001) in the LED's then go online. Connecting the loop pins will cause self test to, if no error is found, continously repeat self test, or if an error is found, to re-attempt the failing test until it passes.

Self Test Switch	Loop Pins	No error	Error
off	off	One pass of the default test, then go online.	Pause 20 displaying error number, then online.
off	on	Repeat self test until loop pin removed. No pause after pass complete.	Pause, then repeat failing test until it passes.
on	off	-- Defines read only self test --	
on	on	-- Defines read only self test --	

8-6. WRITE/READ SELF TEST

The self test with the write/read test appended is selected by holding the write test enable switch in while depressing the self test switch. Caution: this test will destroy data and format the test cylinder. If the self test switch is released, one pass of the write test procedure is executed. If the self test switch is held in, self test will repeat, stepping in one cylinder each pass, until an error is found and then pause until the self test switch is released. Once the self test switch is released the controller will go online. Connecting the loop pins ('on') will cause self test, if no error is found, to repeat the self test with the write and read test appended over after stepping in one cylinder. If an

error is found self test will display the test number and, if the self test switch is depressed, stop until the self test switch is released, else, loop on the failing test until it passes.

WRITE/READ SELF TEST

Self Test Switch	Loop Pin	No error	Error
off	off	One pass of write/ read self test, pause 10 seconds, then go online.	Pause 20 seconds with error number in LED's, then go online.
off	on	After one pass, step in one cylinder and repeat write/ read test.	Pause, then repeat failing test until it passes.
on	off	After one pass, step in one cylinder and repeat write/ read test. Pause after pass complete.	Pause until self test switch is released, display error number.
on	on	After one pass, step in one cylinder and repeat write/ read test. No pause after pass.	Pause until self test switch is released, display error number.

8-7.

READ ONLY TEST

The self test with the read only test appended is selected by depressing and holding the self test switch in. Note: This test will read the test cylinder (either single or double sided diskette) checking for all errors associated with the read operation. Holding the self test switch in cause self test to loop, stepping the head in one cylinder each pass, reading a cylinder. If no error is found, self test will contine to loop, if an error is found, self test will stop and wait for the self test switch to be released. If the loop pins are connected and no error is found, self test will loop faster, if an error is found, self will repeat the failing test until it passes.

self test switch	Loop Pins	no error	error
off	off	-- Default self test --	
off	on	-- Default self test --	

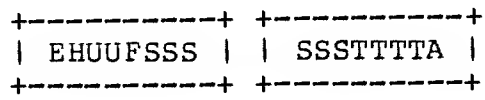
on	off	Repeat complete read only self test. Pause after pass complete.	Stop until self test switch is released, display error number.
on	on	Repeat complete read only self test. No pause after pass complete.	Repeat failing test until it passes.

8-8. SELF TEST ERROR EXPLANATIONS

This section describes how to interpret the results of the self test procedure from either the Return Self Test Results command or from the LED's mounted on the 7902 controller board. Self test is broken into steps called tests and subtest. Each test and subtest has an associated number returned and displayed when an error is encountered during the execution of that step. Both the test and subtest numbers can be read with the Return Self Test Results command, while only the test number is displayed in the LED's on the controller board.

Note: ET #12309 will allow the operator to display the complete 16 bits of self test results from the controller board.

The two bytes read in the Return Self Test Results command have the following format:



The 5 LED's mounted on the 7902 controller board are interpreted during self test as the following:

```
   ABCD*     - Label on controller board stiffener
   ooooo     - LED polypack
-----------
   TTTTA     - Test number
```

Where:

E - ERROR INDICATOR. On if an error was encountered, else off.

H - HEAD NUMBER. Indicates which head the read or write test failed on.

UU - UNIT NUMBER. Indicates which unit or drive the controller had selected at the time of the failure.

F - FORMAT OF OPERATION. Indicates if the controller was in the IBM (0) or HP (1) mode when the test failed.

SSS SSS - SUBTEST NUMBER. Indicates which subtest of the current test failed.

TTTT - TEST NUMBER. Indicates which test failed.

A - "*" LED. This LED is on (lit) only when the controller is performing self test. When off, the

controller is online and ready to accept HP-IB commands.

If there is no error detected, the two bytes returned in "Return Self Test Results" are zero, and a '00001' is displayed on the controller board LED's.

If an error is encountered, the error number is displayed on the LED's and is made available for the "Return Self Test Results" command. The following is an explanation of the possible failing tests. If viewed from the LED's only the current test can be determined and the reasons for the failure could be any one of the subtests.

TEST NUMBER (TTTT) EXPLANATION

0000 - END OF SELF TEST. Self test passed with no errors.

0001 - READ ONLY MEMORY TEST 1. The failure of this test indicates an error in either ROM chip U51 or U61, the MSB for location !FC00 through !FFFF.

Subtest Number Explanation

000 000 - The precomputed checksum for U51 does not compare with the currently computed checksum.

000 001 - The chip in the U51 socket is not the correct chip for that location (!F000).

000 010 - The precomputed checksum for U61 does not compare with the currently computed checksum.

000 011 - The chip in the U61 socket is not the correct chip for that location.

0010 - READ ONLY MEMORY TEST 2. The Failure of this test indicates an error in either ROM chip U52 or U62.

Subtest Number Explanation

000 000 - The precomputed checksum for U52 does not compare with the currently computed checksum.

000 001 - The chip in the U52 socket is not the correct chip for that location.

000 010 - The precomputed checksum for U62 does not compare with the currently computed checksum.

000 011 - The chip in the U62 socket is not the correct chip for that location.

0011 - READ ONLY MEMORY TEST 3. The failure of this test indicates an error in either ROM chip U71 or U81.

Subtest Number Explanation

000 000 - The precomputed checksum for U71 does not compare with the currently computed checksum.

000 001 - The chip in the U71 socket is not the correct chip for that location.

000 010 - The precomputed checksum for U81 does not compare with the currently computed checksum.

000 011 - The chip in the U81 socket is not the correct chip for that location.

0100 - READ ONLY MEMORY TEST 4. The failure of this test indicates an error in either ROM chip U72 or U82.

Subtest Number Explanation

000 000 - The current checksum for U72 does not compare with the precomputed checksum.

000 001 - The chip in the U72 socket is not the correct chip for that location.

000 010 - The current checksum for U82 does not compare with the pre-computed checksum.

000 011 - The chip in the U82 socket is not the correct chip for that location.

0101 - RAM MEMORY TEST 1. The failure of this test indicates an error in the operation of the U111 chip.

0110 - RAM MEMORY TEST 2. The failure of this test indicates an error in the operation of the U121 chip.

0111 - PHI TEST. The failure of this test indicates an error in the operation of the U141 chip.

1000 - CONTROLLER BOARD TEST 1. The failure of this test indicates a problem on the controller board with the operation of the 'overrun' or 'timeout' logic.

Subtest Number Explanation

000 000 - TIME OUT. The failure of this subtest indicates a problem in the 'timeout' logic. The condition being that a 'timeout' is indicated but was not expected.

000 001 - TIME OUT. The failure of this subtest indicates a problem in the 'timeout' logic. The condition being that a 'timeout' is not indicated but was expected.

000 010 - OVERRUN. The failure of this subtest indicates a problem in the 'overrun' logic. The condition being that an 'overrun' is indicated but was not expected.

000 011 - OVERRUN. The failure of this subtest indicates a problem in the 'overrun' logic. The condition being that an 'overrun' is not indicated but was expected.

1001 - CONTROLLER BOARD TEST 2. A failure of this test indicates a problem on the controller board with the 'DLOOP', address mark detect, or the margin error logic.

Subtest Number		Explanation
000 000	-	IBM MODE DATA DLOOP. The failure of this test indicates a problem of the 'DLOOP' operation in the IBM mode. The condition being that the data received was not what was expected.
000 001	-	IBM MODE CLOCK DLOOP. The failure of this test indicates a problem of the 'DLOOP' operation in the IBM mode. The condition being that the clock pattern received was not what was expected.
000 010	-	HP MODE DATA DLOOP. The failure of this test indicates a problem of the 'DLOOP' operation in the HP mode. The condition being that the data pattern received was not what was expected.
000 011	-	HP MODE CLOCK DLOOP. The failure of this test indicates a problem of the 'DLOOP' operation in the HP mode. The condition being that the clock pattern received was not what was expected.
000 100	-	ADDRESS MARK DETECT. The failure of this subtest indicates a problem in the address mark detect ('AMDT') logic. The condition being that an address mark was indicated but was not expected.
000 101	-	ADDRESS MARK DETECT. The failure of this subtest indicates a problem in the address mark detect ('AMDT') logic. The condition being that an address mark was not indicated when expected.

000 110 - MARGIN ERROR. The failure of this subtest indicates a problem in the margin error logic. The condition being that a margin error was indicated but was not expected.

000 111 - MARGIN ERROR. The failure of this subtest indicates a problem in the margin error logic. The condition being that a margin error was not indicated when expected.

1010 - CONTROLLER BOARD TEST 3. The failure of this test indicates a problem on the controller board with the CRC logic.

Subtest Number Explanation

000 000 - CRC. The failure of this test indicates a problem in the CRC logic. The condition being that a CRC error was not indicated when expected.

000 001 - CRC DLOOP. The failure of this test indicates a problem in the CRC logic. The condition being that the received CRC value was not the expected value.

000 010 - CRC. The failure of this test indicates a problem in the CRC logic. The condition being that CRC error was indicated when not expected.

1011 - DRIVE BOARD TEST. A failure in this test indicates that a problem asscciated with the drive board, drive or controller/drive logic.

Subtest Number Explanation

000 000 - ILLEGAL DRIVE STATUS. The failure of this test indicates that there is a problem with the 'READY' and/or 'LSPIN' signals from the drive board. The condition being that spinning is indicated but ready is not.

000 001 - HEAD DELAY. The failure of this subtest indicates a problem with the head and phase load delay logic. The condition being that there was no delay, or that the delay was less then .5 seconds.

000 010 - HEAD DELAY. The failure of this subtest indicates a problem with the head and phase load delay logic. The condition being that the delay was longer than 2.25 seconds.

000 011 - SEEK. The failure of this subtest indicates a problem in the seek logic. The condition being that after 100 steps toward track 0 there was no track 0 indicator found.

000 100 - TRACK 0 INDICATOR. The failure of this test indicates a problem with the track 0 indicator logic. The condition being that the track 0 indicator was on at a phase other then phase 0 when the actuator was being stepped out.

000 101 - SEEK. The failure of this subtest indicates a problem with the seek logic. The condition being that the track 0 indicator was on when not expected as the actuator was being stepped in.

000 110 - SEEK. The failure of this subtest indicates a problem with the seek logic. The condition being that the track 0 indicator was not on when expected.

000 111 - NO DRIVES. The failure of this test indicates that no drives were found connected to the controller. This may or may not be an error.

1100 - DRIVE TEST. The failure of this test indicates a problem with the rotational timing of the diskette in the indicated drive. Note: This test will only be performed if there is a diskette present in the drive.

Subtest Number	Explanation
000 000	- NO INDEX MARK. The failure of this test indicates that the drive, through status, indicated that a diskette was present and spinning, but, no index mark was found.
000 001	- SPEED. This subtest indicates that the diskette was spinning faster then specified limits.
000 010	- SPEED. This subtest indicates that the diskette was spinning slower then specified limits.
000 011	- SPEED (IBM). This subtest indicates that the diskette was spinning faster than specification allows in IBM format.
000 100	- SPEED (IBM). This subtest indicates that the diskette was spinning slower than specification allows in IBM format.

1101 - WRITE TEST. The failure of this test indicates a problem with recording data or formatting the diskette in the indicated drive. Note: this test is only executed if the write test was selected during the initiation phase.

000 000	- NOT READY. The failure of this subtest indicates that the selected drive is not ready. A drive with a single sided diskette could cause this error.
000 001	- NO DISKETTE. This test would fail if the selected drive indicated that there was no diskette inserted in the drive or that the door is not closed.

000 010 - WRITE PROTECTED. The failure of this test indicates that the status from the selected drive shows the diskette as write protected.

1110 - READ TEST. The failure of this test indicates a problem in reading data from the diskette. This may result in a failure to write or read correctly or bad media.

000 000 - NOT READY. The failure of this subtest indicates that the selected drive is not ready. i.e., maybe the diskette has been removed.

000 001 - BAD ID FIELD. The failure of this subtest indicates that current ID field contained misinformation.

000 010 - NO ID FIELDS FOUND. The failure of this subtest indicates that no ID fields were found after 2 revolutions of the diskette.

000 011 - WRONG ID FIELD. The failure of this subtest indicates that during the current read, some ID fields were found but the target ID field was not.

000 100 - NO DATA MARK. The failure of this subtest indicates that during the current read, the target ID field was found but the corresponding data mark was not found.

000 101 - CRC ERROR. The failure of this subtest indicates that the current data field contained a CRC error.

000 110 - OVERRUN. The failure of this subtest indicates that an overrun error occurred in the current read attempt.

000 111 - DATA MISCOMPARE. The failure of this test indicates that the status indicates a 'good' read but the read data does not compare with the expected value.

001 000 - SEEK NOT READY. This failure indicates that the drive is not ready during the logical seek operation. This subtest is only executed if the read only test is selected.

001 001 - UNKNOWN FORMAT. This test is only executed during the read only self test. Its failure indicates that the controller is unable to determine the format of the diskette in the indicated drive.

001 010 - SEEK FAILURE. The failure of this subtest indicates that the logical seek algorithim could not find the target track.

1111 - SLP FAILURE. The failure of this test indicates that the basic operation of the MCC, PHI or RAM logic does not funtion correctly.

000 000 - INITIALIZATION. This is the first test executed by the controller. It is not a test in the true sense but only an attempt to change the LEDs to signal the operator that the self test procedure has begun.

000 001 - PROCESSOR FAULT. The failure of this test indicates that the MCC, chip U131, or chips U81 or U82 (ROM memory or self test) are not working correctly.

000 010 - SLP FAULT. The failure of this subtest indicates that either the MCC (U131), ROM (U81 or U82), or RAM (U111 or U121) are not working correctly.

SECTION IX
REMOVAL AND REPLACEMENT

9-1. INTRODUCTION

This section provides detailed removal and replacement procedures for those disc drive assemblies that are field replaceable. The order of presentation is based on which assemblies are most often removed or replaced before another assembly can be removed. Throughout the procedures references are made to index and figure numbers (those numbers in parentheses) which correspond to illustrations found in section X of this manual. A figure number is listed with an index number when an illustration is first referenced and it remains in effect until a new illustration is referenced.

A procedure is presented early in this section for removing power from the disc drive since power must be removed before any of the assemblies can be removed.

Adjustments and/or checks must be performed following the replacement or movement of certain items in the disc drive. These items, and the required adjustments and checks, are detailed in table 9-1.

WARNING

The information given in this section is for service-trained personnel only. To avoid potentially serious electrical shock, do not proceed further in this section unless qualified to do so.

Table 9-1. Adjustments/Checks Required Following Component Replacement

COMPONENT	ADJUSTMENT/CHECK
Write Protect Detector	Write protect detector adjustment procedure. Refer to paragraph 9-12.
Head Load Actuator	Head load actuator adjustment procedure. Refer to paragraph 9-15. Head load actuator timing check. Refer to paragraph 9-16.
Sector/Index Phototransistor	Sector/index phototransistor adjustment procedure. Refer to paragraph 9-19.
Sector/Index LED	Sector/index phototransistor adjustment procedure. Refer to paragraph 9-19.
Track 0 Detector	Track 0 detector adjustment procedure. Refer to paragraph 9-23.

9-2. POWER REMOVAL AND RESTORATION

Most of the removal and replacement procedures given in this section require that the disc drive power be removed before they are performed. To remove power from the disc drive, proceed as follows:

a. Set the power switch on the host system to OFF.

b. Disconnect the cables from the following connectors on the disc drive:

- J5 (4, figure 10-1).
- AC power connector (7, figure 10-3).

Power is restored to the disc drive by reversing this procedure.

9-3. CONNECTOR P2 PIN EXTRACTION

Certain of the removal and replacement procedures require that pins (and attached wires) be extracted from connector P2 (6, figure 10-1). To remove a pin from connector P2, proceed as follows:

a. At the front of connector P2, insert the end of a pin extractor tool (or the end of a paper clip) between the desired pin and the wall of the connector. See figure 9-1.

b. Push down on the pin extractor to release the locking spring on the pin.

c. Remove the pin by pulling on attached wire from the rear of the connector.

To replace a pin in connector P2, push the pin into the appropriate opening at the rear of the connector until it locks in place.

Note: Repeated extractions of a pin will flatten the locking spring and prevent the pin from locking into the connector. When this occurs, carefully bend the spring forward until its locking action is restored.

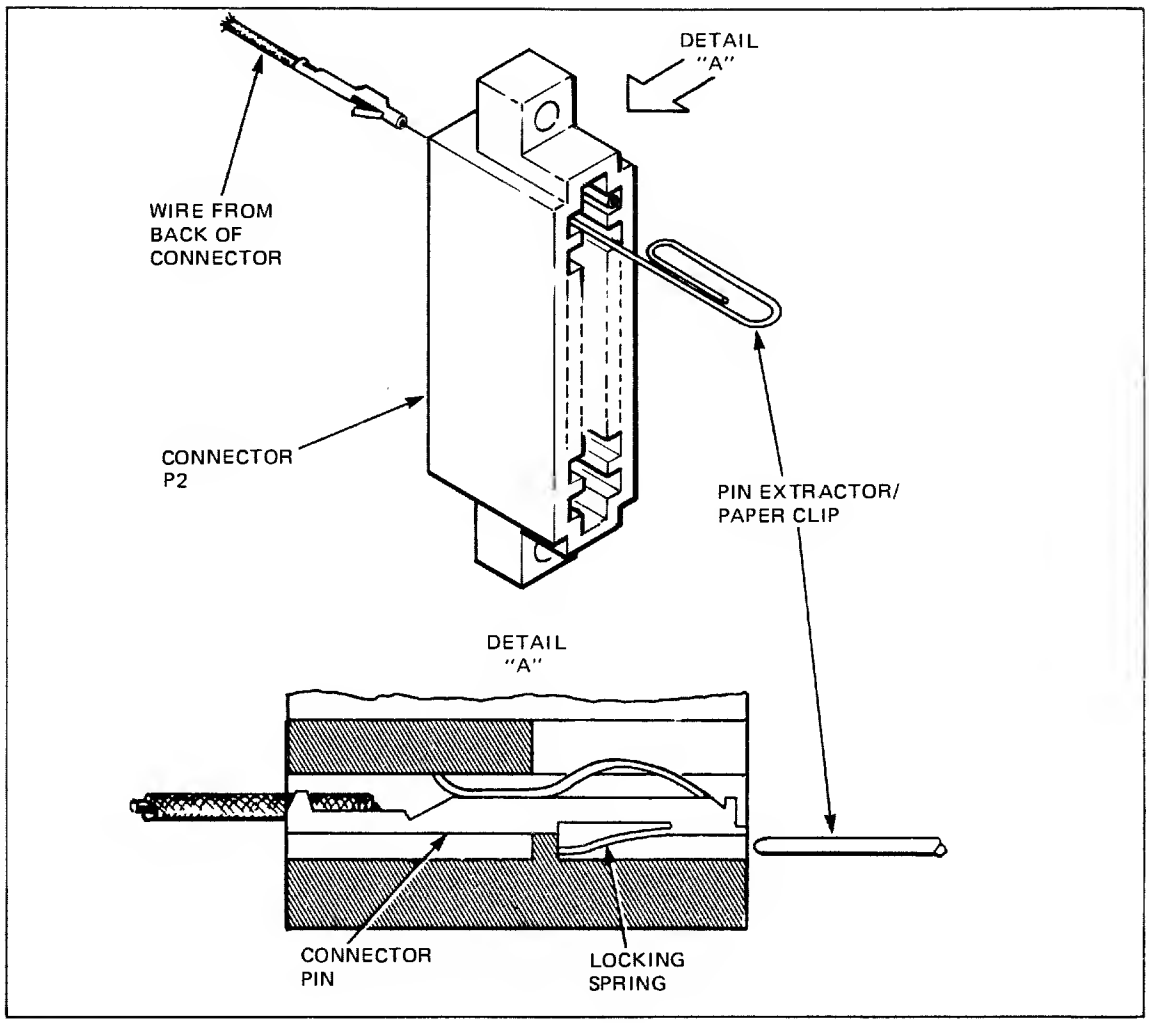
9-4. DRIVE PCA

The drive PCA (1, figure 10-1) is removed from the disc drive as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Disconnect the cables from the following connectors on the drive PCA:

- J1 (2, figure 10-1)
- J3 (14)
- J6 (7)
- J7 (3)



7310-18

Figure 9-1. Connector P2 Pin Extraction

c. Remove four screws (5) securing the drive PCA to the disc drive frame.

d. Disconnect the cable from connector J2 (6) on the drive PCA and remove the PCA from the disc drive.

The drive PCA is installed by reversing this procedure. Ensure that all of the connectors removed in steps b and d are firmly connected to the PCA.

9-5. HEAD COVER SHIELD

The head cover shield (11, figure 10-3) is removed from the disc drive as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Loosen the two screws securing the head cover shield to the guide opening assembly (2, figure 10-5).

c. Move the head cover shield towards the head assembly until the shield is free of the two retaining screws.

d. Remove the head cover assembly from the disc drive.

The head cover shield is installed by reversing this procedure.

9-6. CARTRIDGE GUIDE

9-7. CARTRIDGE GUIDE ACCESS

The cartridge guide assembly (12, figure 10-3) swings open to provide access to certain components mounted on the cartridge guide and the frame of the disc drive. To swing open the cartridge guide, proceed as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Remove the head cover shield as described in paragraph 9-5.

c. Position the read/write heads to approximately track 0 by turning the stepper actuator shaft (8, figure 10-4) fully counterclockwise.

d. Unlatch the cartridge guide assembly by pressing the push bar (11, figure 10-1) on the front of the drive.

CAUTION

The heads should never touch each other. Always insert a piece of clean lens tissue between the heads when the head load bail is disengaged from the head load arm.

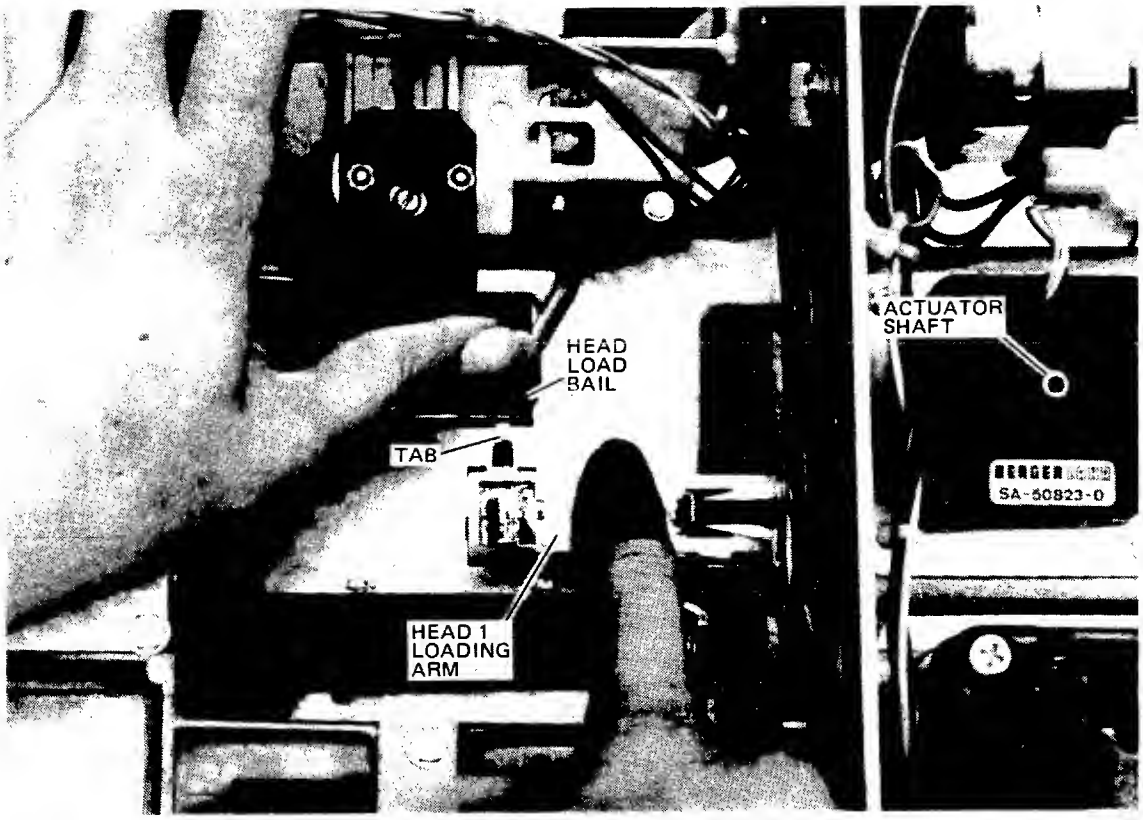
e. Refer to figure 9-2A. Carefully hold the movable arm of head 1 with one finger while pushing the head load bail up and back until the tab on the movable arm clears the head load bail. Be sure that the bail clears the head load arm before releasing the bail.

f. Insert a clean piece of lens tissue between the lower and upper heads to prevent them from touching and then gently release (lower) the movable arm of head 1.

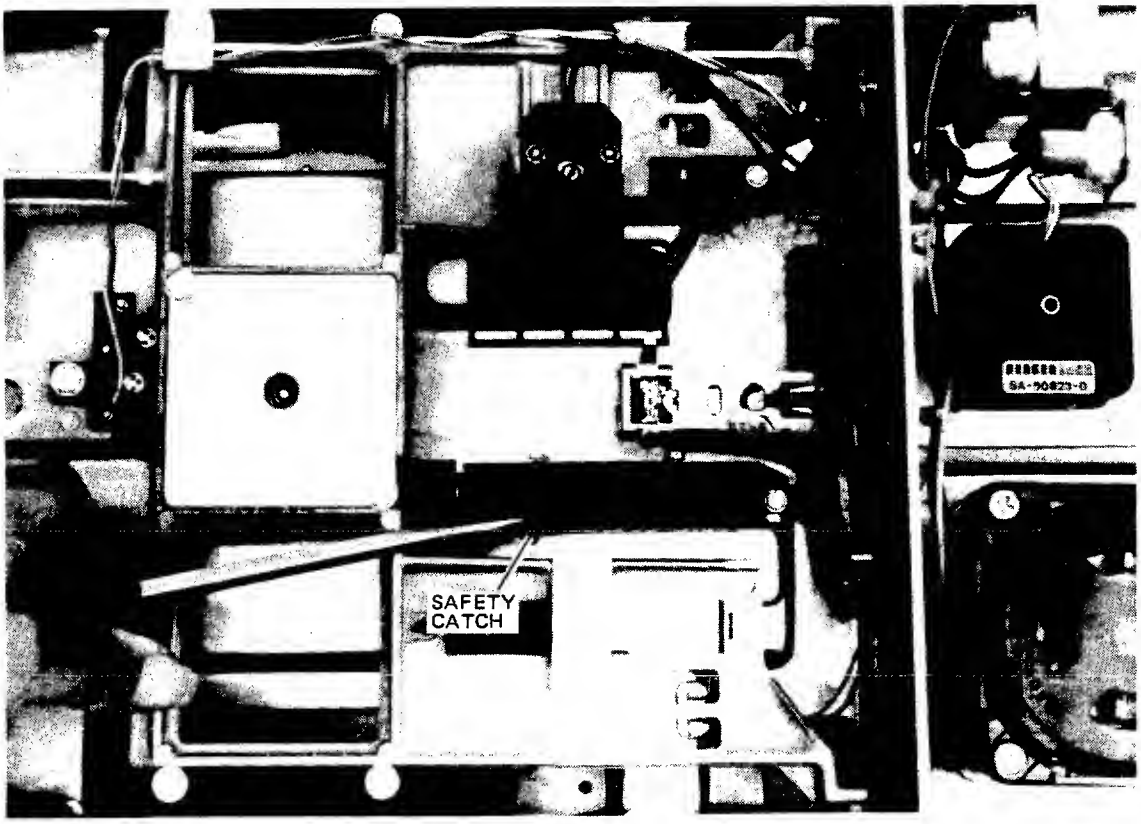
g. Loosen the two screws (13, figure 10-3) securing the door latch plate to the cartridge guide assembly.

h. Refer to figure 9-2B. Release the safety catch on the guide opening assembly by pressing the catch towards the rear of the drive. When the catch is released, swing the cartridge guide assembly up and away from the frame of the disc drive, as illustrated in figure 10-5.

The cartridge guide assembly is restored to its normal operating position by reversing this procedure. Following restoration to normal operation, perform the cartridge guide assembly adjustment procedure described in paragraph 9-8.



A. HEAD UNLOADING



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B. SAFETY CATCH RELEASE

Figure 9-2. Cartridge Guide Access Details

9-8. CARTRIDGE GUIDE ADJUSTMENT

To check the adjustment of the cartridge guide assembly, proceed as follows:

a. Insert end no. 2 of cartridge guide adjustment tool, part no. 1150-1310, through the cartridge guide tool hole (4, figure 10-4) and screw it completely into the disc drive frame. Hand tighten the tool.

b. Move the door handle (9, figure 10-1) into the latched position and hold it tightly against the latch.

c. Tighten the two screws (13, figure 10-3) securing the cartridge guide to the latch plate.

d. Remove the tool and check to determine if the flange on the clamp hub clears the cartridge guide when the spindle is rotating. If the clamp hub rubs on the cartridge guide, repeat steps a through c.

e. Adjust the cartridge guide stop so that it is within 0.005 inch of the disc drive frame.

f. Insert a flexible disc into the drive, close and open the door, and check for proper operation.

g. Following the completion of this adjustment procedure, perform the following procedures:

- Sector/Index Phototransistor Adjustment Procedure, paragraph 9-19.
- Write Protect Detector Adjustment Procedure, paragraph 9-12.
- Head Load Actuator Adjustment Procedure, paragraph 9-15.

9-9. SECTOR/INDEX LED

The sector/index LED assembly (1, figure 10-4) is removed from the disc drive as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Note the color coding of the two wires attached to the sector/index LED assembly and then unsolder the wires.

c. Remove the screw securing the sector/index LED assembly to the cartridge guide assembly (12, figure 10-3) and remove the LED assembly.

The sector/index LED assembly is replaced by reversing this procedure. Following installation, perform the sector/index phototransistor adjustment procedure described in paragraph 9-19.

9-10. WRITE PROTECT DETECTOR

9-11. WRITE PROTECT DETECTOR REMOVAL

The write protect detector assembly (2, figure 10-4) is removed from the disc drive as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Remove the drive PCA as described in paragraph 9-4.

c. Extract the following pins from connector P2 (6, figure 10-1):

Pin	Wire
4	red
D	black
11	white
M	gray

d. Remove the screw securing cable clamp (5, figure 10-4) to the disc drive frame.

e. Remove the screw securing the write protect detector assembly bracket to the disc drive frame and remove the detector assembly.

The write protect detector assembly is installed by reversing this procedure. Following installation, perform the write protect detector adjustment procedure described in paragraph 9-12.

9-12. WRITE PROTECT DETECTOR ADJUSTMENT

To check the adjustment of the write protect detector assembly, proceed as follows:

a. Restore power to the disc drive as described in paragraph 9-2.

b. Insert a flexible disc having an open write protect notch (or hole) into the disc drive.

c. Using a 10:1 probe, connect an oscilloscope to the WPRTH test point on the drive PCA. Use drive PCA GND 1 test point for signal ground.

Note: All oscilloscope sensitivity settings given in this section assume the use of 10:1 oscilloscope probes. If 1:1 probes are used, the sensitivity settings should be scaled accordingly.

d. Set the oscilloscope controls as follows:

Sweep — 2 msec/div
Sensitivity — 0.1 volt/div
Input — DC
Trigger — INT, DC
Display —A

e. Slightly loosen the screw securing the write protect detector assembly bracket to the disc drive.

f. Adjust the position of the write protect detector assembly until the waveform observed on the oscilloscope is at maximum amplitude. Tighten the screw loosened in step e.

g. Check that the position of the write protect detector does not restrict insertion of a flexible disc into the disc drive. If necessary repeat steps e and f above.

9-13. HEAD LOAD ACTUATOR

9-14. HEAD LOAD ACTUATOR REMOVAL

The head load actuator assembly (2, figure 10-3) is removed from the disc drive as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Remove the head cover shield (11, figure 10-3) as described in paragraph 9-5.

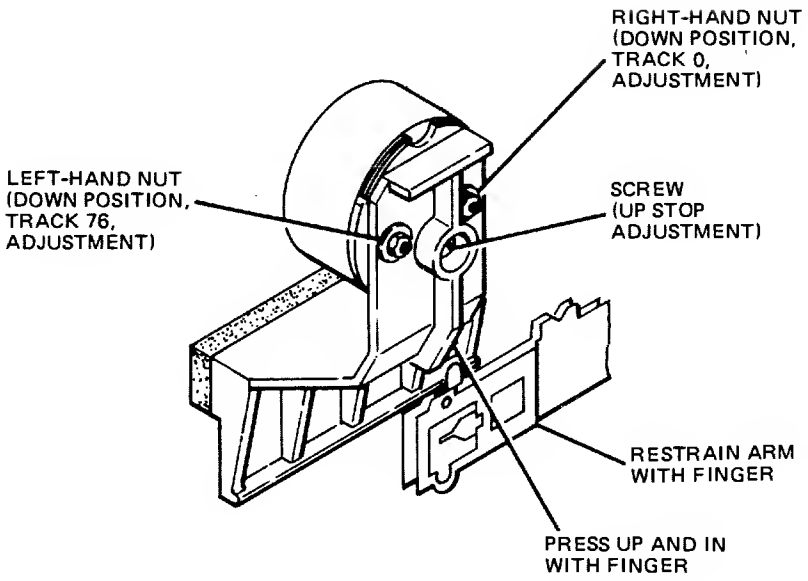
c. Extract the following pins from connector P2 (6, figure 10-1):

Pin	Wire
17	black
U	black

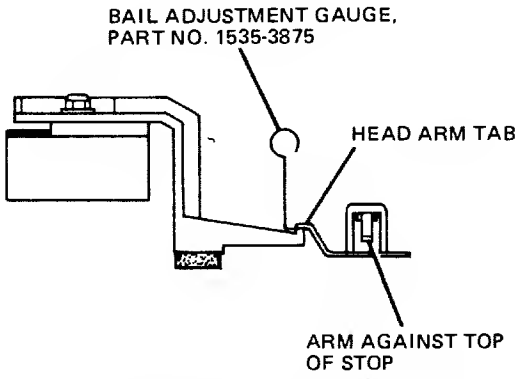
d. Swing open the cartridge guide assembly as described in paragraph 9-7.

e. Remove the screw securing the head load actuator to the cartridge guide assembly.

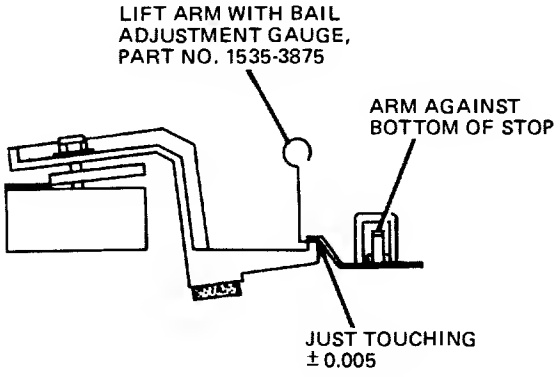
The head load actuator is installed by reversing this procedure. Hold the actuator in the position shown in figure 9-3A when tightening its mounting screw. Do not install the head load shield at this time. Following installation of the actuator, perform the head load actuator adjustment procedure described in paragraph 9-15 and the timing check described in paragraph 9-16.



A. ADJUSTMENT CONTROLS AND UNLOADING DETAILS



B. DOWN POSITION ADJUSTMENT



C. UP POSITION ADJUSTMENT

7310-20

Figure 9-3. Head Load Actuator Unloading and Adjustment Details

9-15. HEAD LOAD ACTUATOR ADJUSTMENT

To check the adjustment of the head load actuator assembly, proceed as follows:

a. Restore power to the disc drive as described in paragraph 9-2.

b. Position the heads to approximately track 0.

c. Insert a flexible disc into the disc drive and energize the head load actuator coil by selecting the drive.

d. The down position of the head load actuator bail is adjusted with two self-locking nuts that secure the bail to the actuator. These nuts are illustrated in figure 9-3A.

e. With the read/write heads at track 0, adjust the right-hand nut until the tip of bail adjustment gauge, part no. 1535-3875, just fits between the bail and the tab on the head 1 movable arm. See figure 9-3B.

f. Position the heads at track 76 and repeat step e, this time adjusting the left-hand nut.

g. Return to track 0 and recheck the clearance. If necessary, readjust the setting of the right-hand nut.

h. Continue to check the clearance at track 0 and track 76 until both are correct.

i. Deselect the drive and open the cartridge guide assembly by pressing the push bar on the front panel of the drive.

j. Refer to figure 9-3C. With the loop of the bail adjustment tool hooked over the tip of the load arm tab, carefully pull the arm out to its maximum travel (do not flex the arm).

k. Adjust the up stop adjustment screw until the bail just contacts the tab of the head load arm. It may be necessary to first adjust the screw too far in and then back it off, as required.

l. Following the adjustment, ensure that there is clearance between the disc and the outside head when a flexible disc is inserted into the drive.

9-16. HEAD LOAD ACTUATOR TIMING CHECK

To check the timing of the head load actuator, proceed as follows:

a. Restore power to the disc drive as described in paragraph 9-2.

b. Insert a flexible disc into the disc drive. Select head 0 and step to track 0. Write a series of 0's on the disc.

c. Using 10:1 probes, connect an oscilloscope to the following test points on the drive PCA:

Channel A — PREAMP +
Channel B — PREAMP –

Use test point HDLDL on the drive PCA for oscilloscope sync and test point GND 3 for signal ground.

d. Set the oscilloscope controls as follows:

Sweep — 10 msec/div
Sensitivity — 0.01 volt/div
Input — DC
Trigger — EXT, –, DC, NORM, SINGLE
Display — A + B, B INV

e. Observe the read signal on the oscilloscope. The signal should reach 50% of full amplitude in 35 milliseconds or less. See figure 9-4. If this is not the case, proceed with the remainder of this procedure.

f. Repeat the head load actuator adjustment procedure described in paragraph 9-15.

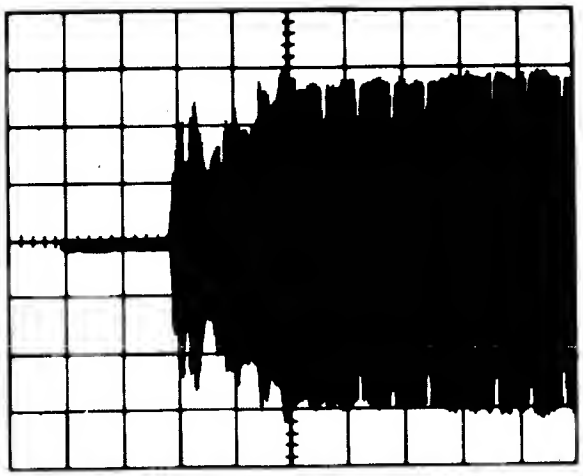


Figure 9-4. Head Load Actuator Timing Check Waveform

CAUTION

Do not adjust the head load actuator up stop adjustment screw more than 1/4-turn clockwise.

g. Repeat step e. If the timing is still not correct, adjust the head load actuator up stop adjustment screw clockwise until the timing is correct. The up stop adjustment screw is shown in figure 9-3A.

9-17. SECTOR/INDEX PHOTOTRANSISTOR

9-18. SECTOR/INDEX PHOTOTRANSISTOR REMOVAL

The sector/index phototransistor assembly (4, figure 10-2) is removed from the disc drive as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Disconnect connector P2 (6, figure 10-1) from the drive PCA.

c. Detach the following wires from the door closed switch (3, figure 10-2):

Switch Contact	Wire
Common	orange
N/C	gray
N/O	red

d. Extract the following wires from connector P2 (6, figure 10-1):

Pin	Wire
12	black
N	green
P	brown
6	orange
F	gray
H	red

e. Remove the screw securing cable clamp (10, figure 10-2) to the frame of the drive.

f. Remove the sector/index phototransistor assembly from the disc drive.

The sector/index phototransistor assembly is installed by reversing this procedure. Following installation perform the sector/index phototransistor adjustment procedure described in paragraph 9-19.

9-19. SECTOR/INDEX PHOTOTRANSISTOR ADJUSTMENT

To check the adjustment of the sector/index phototransistor assembly, proceed as follows:

a. Restore power to the disc drive as described in paragraph 9-2.

b. Insert double-sided alignment disc, part no. 9164-0111, into the disc drive and close the door.

c. Using 10:1 probes, connect an oscilloscope to test point INDEX H on the drive PCA.

d. Set the oscilloscope controls as follows:

Sweep – 2 msec/div

Sensitivity – 0.2 volt/div

Input – DC

Trigger – INT, +, DC, NORM

Display – A

e. Check that two pulses are present as shown in the figure. The amplitude of the pulses should be approximately 4.0 volts. If the two pulses are not correct, proceed to step f and attempt to obtain the correct signal. If it is correct, the procedure is complete.

f. Loosen the screw securing the sector/index phototransistor assembly until the assembly can just be moved.

g. Adjust the position of the sector/index phototransistor assembly until the oscilloscope waveform agrees with step e.

h. Tighten the sector/index transistor assembly retaining screw and check that the waveform is still acceptable.

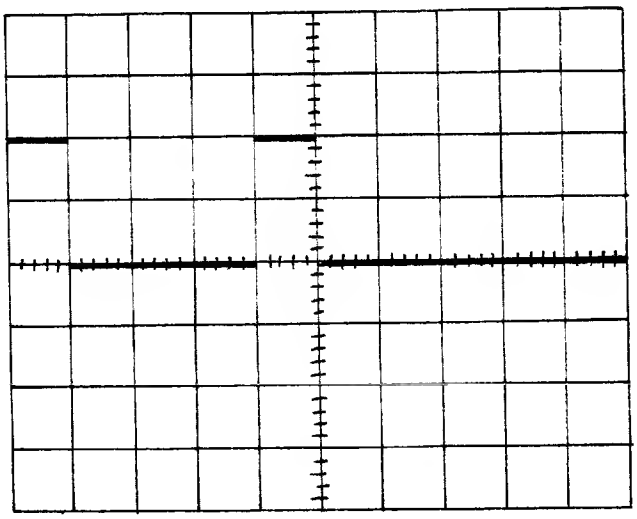


Figure 9-5: Index Pulse Waveform

9-20. TRACK 0 DETECTOR

9-21. TRACK 0 DETECTOR REMOVAL

The track 0 detector (5, figure 10-5) is removed from the disc drive as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Manually rotate the stepper actuator shaft (8, figure 10-4) fully clockwise to track 77.

c. Remove the screw securing the track 0 detector bracket to the frame of the disc drive and remove the track 0 detector assembly.

d. Remove the drive PCA from the disc drive as described in paragraph 9-4.

e. Extract the following pins from connector P2 (6, figure 10-1):

Pin	Wire
3	brown
C	black
O	orange
L	red

f. Remove the screw securing cable clamp (5, figure 10-4) to the disc drive.

g. Remove the track 0 detector from the disc drive.

The track 0 detector is installed by reversing this procedure. Following installation, perform the track 0 detector adjustment procedure described in paragraph 9-23.

9-22. TRACK 0/76 STOP ADJUSTMENT

This adjustment is not field adjustable.

9-23. TRACK 0 DETECTOR ADJUSTMENT

To check that the track 0 detector is correctly adjusted, proceed as follows:

a. Before performing this procedure, check the head radial alignment (paragraph 7-17) and adjust if necessary.

b. Insert the alignment disc into the disc drive.

c. Loosen the screw securing the track 0 detector and move the detector back as far as possible towards the actuator assembly. Tighten the securing screw.

d. Recalibrate the disc drive by pressing the RESET pushbutton on the DSU.

e. Using 10:1 probes, connect an oscilloscope to the following points on the drive PCA:

Channel A — PREAMP +
Channel B — PREAMP –

f. Use test point INDEX H on the drive PCA for oscilloscope sync and test point GND 3 for signal ground.

g. Set the oscilloscope controls as follows:

Sweep — 20 msec/div
Sensitivity — 0.01 volt/div
Input — DC
Trigger — EXT, –, DC, NORM
Display — A + B, B INV

h. Using the DSU, step the carriage assembly in until the data burst recorded on track 0 is visible.

i. Loosen the screw securing the track 0 detector and move the detector forward until the TRACK 0 LED on the DSU lights. Tighten the securing screw.

j. Using a 10:1 probe, connect the oscilloscope to drive PCA test point TK0H. Use drive PCA GND 1 test point for signal ground. Set oscilloscope for a vertical deflection of 0.1 volt/div, continuous sweep.

k. Check that voltage level at TK0H test point is high (+5 volts).

l. If the voltage is not high, loosen the screw securing the track 0 detector. Move the detector forward towards the spindle until the TK0H test point goes high.

m. Step the carriage to track 02. Check that the TK0H test point goes low. If this is not the case, move the track 0 detector back towards the actuator assembly.

n. Recheck the adjustment by stepping the heads between tracks 01 and 02. Check that TK0H test point is low at track 02 and high at track 01. A perfect adjustment presents a squarewave on the oscilloscope.

9-24. FRONT PLATE

The front plate assembly is removed from the disc drive as follows:

a. Remove power from the disc drive as described in paragraph 9-2.

b. Insert the cartridge guide adjustment tool through the cartridge guide tool hole (4, figure 10-4) in the cartridge guide assembly (12, figure 10-3) and screw it into the disc drive frame. Hand tighten the tool.

c. Remove the following pins from connector P2 (6, figure 10-1):

Pin	Wire
2	black
B	brown
9	blue
K	purple

d. Remove the screw securing cable clamp (9, figure 10-2) and remove the clamp.

e. Remove the two Allen-head screws securing the handle to the front plate and remove the handle.

f. Remove the two screws securing the lock plate assembly to the front plate.

The front plate is installed by reversing this procedure. Following replacement, perform the sector/index phototransistor adjustment procedure described in paragraph 9-19.

9-25. LOCK PLATE ASSEMBLY

The lock plate assembly (17, figure 10-1) is removed from the disc drive as follows:

a. Perform the front plate removal procedure as described in paragraph 9-24.

b. Remove the lock plate assembly from the disc drive.

The lock plate assembly is replaced by reversing this procedure. Following installation, adjustment of the door lock solenoid (10) should not be necessary. If adjustment is required, the gap between the armature tab and the latch should be 0.15 ± 0.010 inch. The adjustment can be made by loosening the two screws on the armature.

SECTION X
REPLACEABLE PARTS

10-1. INTRODUCTION

This section provides a listing of all field-replaceable parts for the HP 7902 Disc Drive and an illustrated parts breakdown for the 07902-60025 disc drive assembly, as well as replacement part ordering information. Replacement parts for the HP 7902 are listed in table 10-1; an illustrated parts breakdown for the 07902-60025 disc drive is provided in figures 10-1 through 10-5.

The parts listing lists the following information for each part:

- FIG. & INDEX NO. The figure and index number which indicates where the replacement part is illustrated.
- HP PART NO. The Hewlett-Packard part number for each replaceable part.
- DESCRIPTION. The description of each replaceable part.
- UNITS PER ASSEMBLY. The total quantity of each part used in the major assembly.

10-2. ORDERING INFORMATION

To order replaceable parts for the disc drive, address the order to your local Hewlett-Packard Sales and Service Office. Sales and Service Offices are listed at the back of this document. Specify the following information for each part ordered:

- Model and full serial number.

- Hewlett-Packard part number.

- Complete description of each part as provided in the replaceable parts listing.

Table 10-1. HP 7902A Replaceable Parts

FIGURE & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSEMBLY
10-1	07902-60025	Disc Drive Assembly*	1
10-1, 1	07902-60023	Drive PCA-A2	1
8	1535-3652	Door Closed Switch	1
17	1535-3874	Lock Plate Assembly	1
10-2, 4	1535-3872	Sector/Index Phototransistor Assembly	1
7	1535-3651	Drive Belt, 60 Hz	1
—	1535-3649	Drive Belt, 50 Hz	
10-3, 2	1535-3870	Head Load Actuator	1
10-4, 1	1535-3871	Sector/Index LED Assembly	1
2	1150-1309	Write Protect Detector Assembly	1
10-5, 5	1535-3873	Track 0 Detector Assembly	1
—	07902-60024	Controller PCA-A1	1
—	9164-0096	Flexible Disc, Double-Sided, Unformatted	
—	5061-1395	Flexible Disc, Single-Sided, Unformatted	
		*Disc Drive Assembly part number is 07902-60038 when included with re-usable shipping container.	

Manual Part No. 07902-900600

Printed in U.S.A.
November 1978